



A885GM-M2

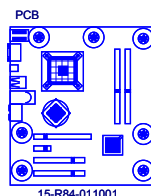
Rev:1.0

SCHEMATICS TABLE:

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| 17 | PCI-E Slot(X16,X1) | | |

REVISION HISTORY:

| Rev | Date | Notes |
|-----|------------|---|
| A | 2009-12-22 | INITIAL RELEASE Change from A785GM-M7 V:A |
| 1.0 | 2010-02-25 | Change to V1.0 1. RN18 pull high to VCC_DUAL_F page 27 2. ER37 change to 11K-1-04 for USB EYE page 19 3. RTC issue fix. C164,C166 change to 27pF. page 20 4. ER41 change to 1.91K-1-04,ER40 change to 1.05K-1-04.R191 change to 19.1K-1-04 for OCP set . page 6 5. R134 change to 30k for Vcore NB OCP by vendor. page 4 6. EC46 change to 270U-16D-OS. page 5 7. RGMII GBE LAN isn't used.direct short to GND. page 21 8. USBCLK not connected by default,del R160,R91. page 19 9. Add D27, is used to prevent the battery runs out for EUP. P18 10. SB change to SB850. P18 |



IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

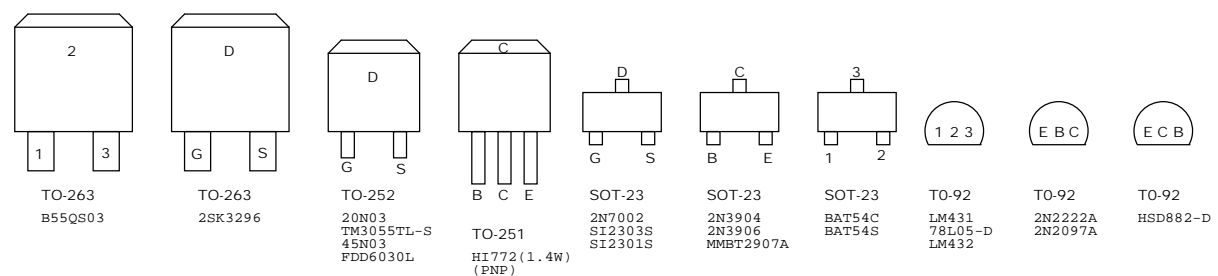
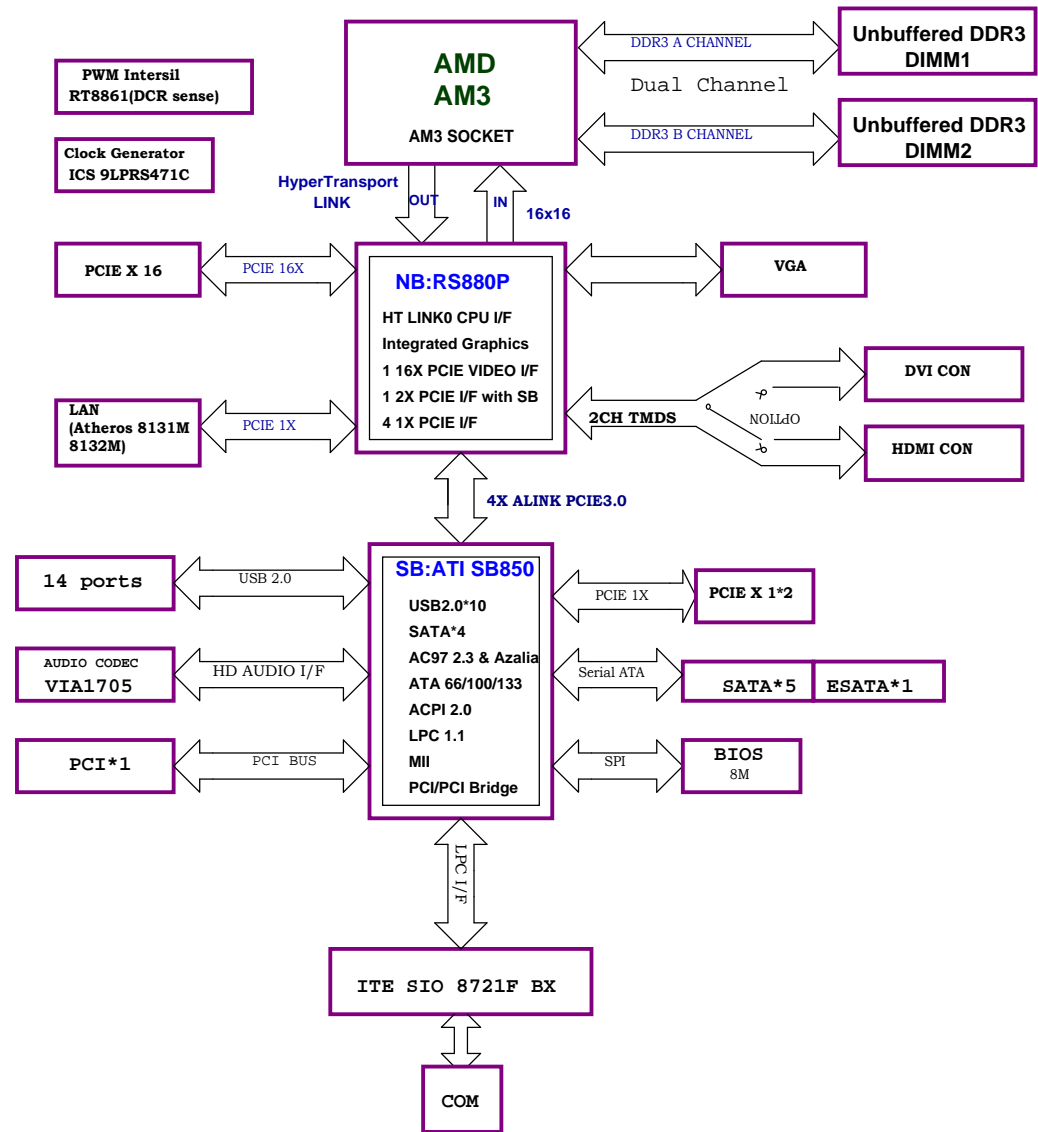
2) DESIGN NOTES in yellow are notes of caution.

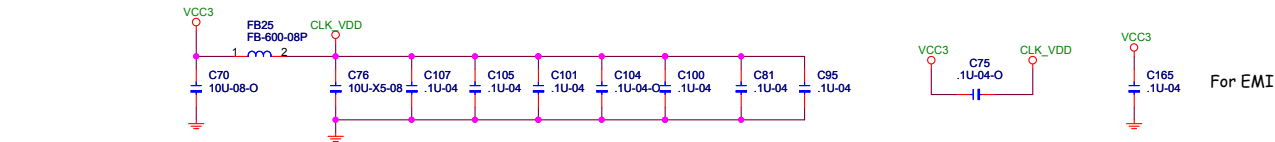


3) DESIGN NOTES in red are critical, and must be understood and followed.

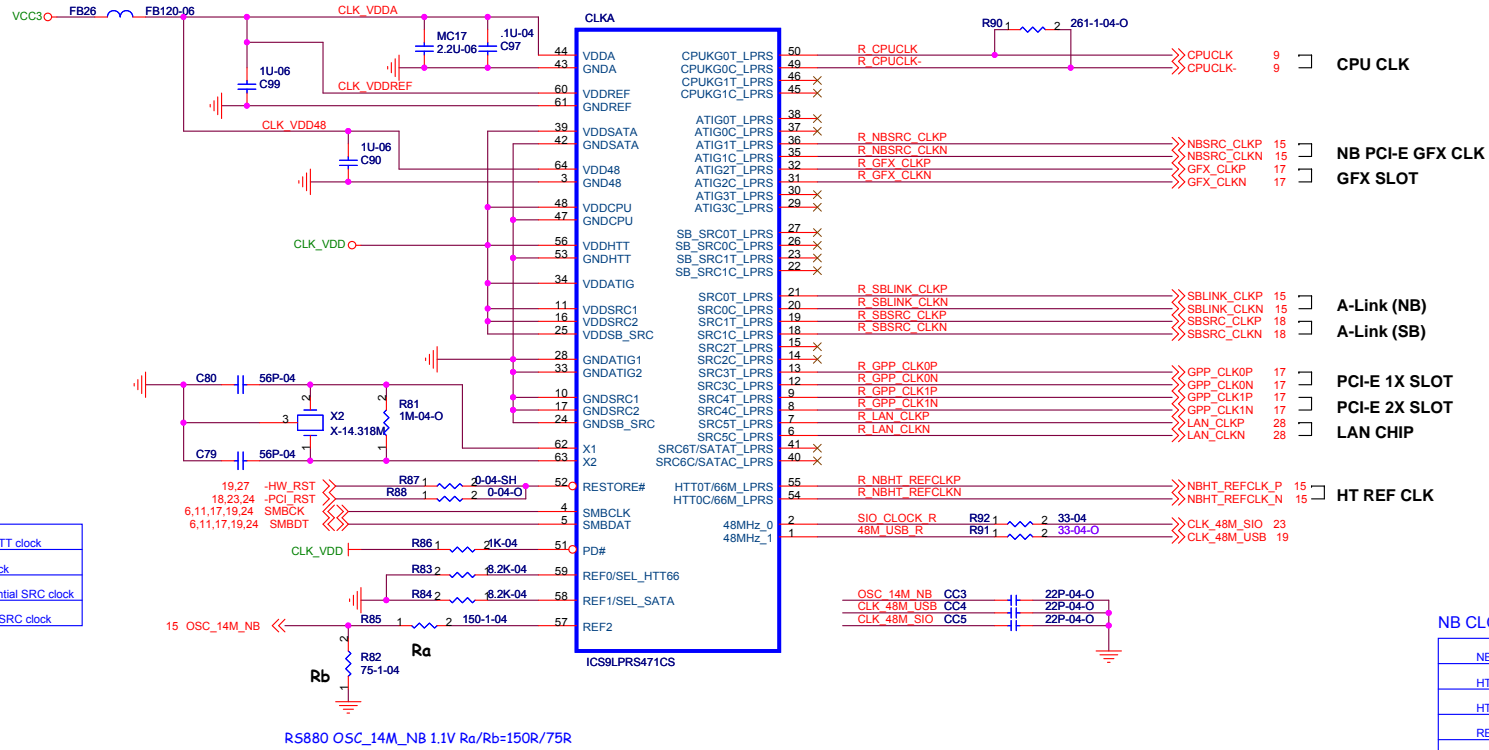
PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

| | | | |
|------------|---------------------------|-----------------------------|---------|
| | | Elitegroup Computer Systems | |
| Title | | | |
| Cover Page | | | |
| Size | Document Number | Rev | |
| Custom | A885GM-M2 | 1.0 | |
| Date: | Friday, February 26, 2010 | Sheet | 1 of 33 |





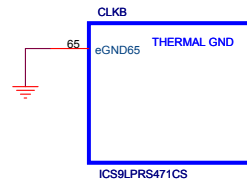
- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO CLOCK GEN
- 2- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



| | | |
|-----------|----|--|
| SEL_HTT66 | 1 | 66 MHz 3.3V single ended HTT clock |
| | 0* | 100 MHz differential HTT clock |
| SEL_SATA | 1 | 100 MHz non-spreading differential SRC clock |
| | 0* | 100 MHz spreading differential SRC clock |

* default

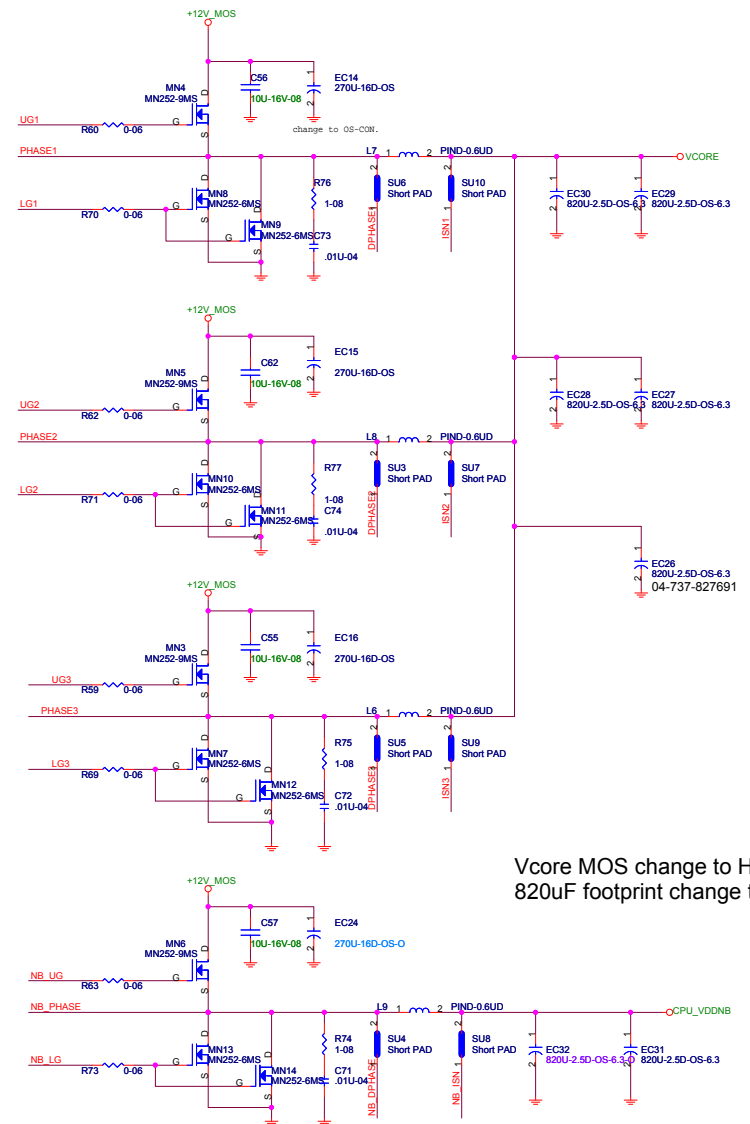
RS880 OSC_14M_NB 1.1V Ra/Rb=150R/75R



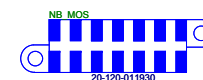
NB CLOCK INPUT TABLE

| | |
|--------------|------------------------|
| NB CLOCKS | RS880 |
| HT_REFCLKP | 100M DIFF |
| HT_REFCLKN | 100M DIFF |
| REFCLK_P | 14M SE (1.1V) |
| REFCLK_N | VREF |
| GFX_REFCLK | 100M DIFF(IN/OUT)* |
| GPP_REFCLK | NC or 100M DIFF OUTPUT |
| GPPSB_REFCLK | 100M DIFF |

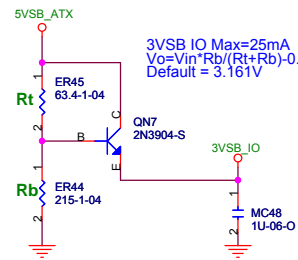
* RS880 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.
Clock chip has internal serial terminations for differential pairs



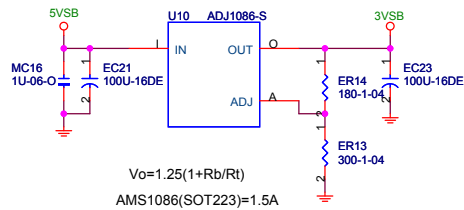
| | RT8855 | RT8861 (new) |
|----|-------------------|--------------------|
| Ca | RT8855PQV | RT8861PQV |
| Cb | R341 1K;R366 NC | R341 30K;R366 6.2K |
| Cc | R367 NC;R368 0ohm | R367 0ohm;R368 NC |
| Cd | R337 33K | R337 12K |
| | | Default |



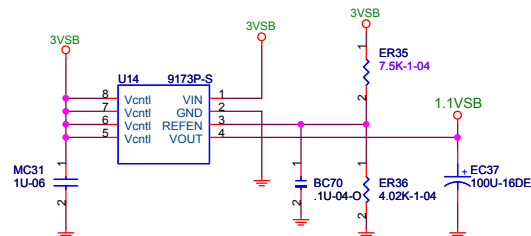
3VSB_IO



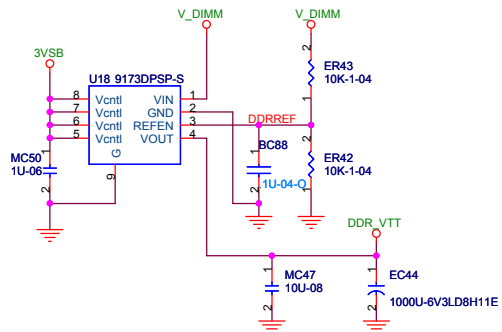
3VSB



1.1VSB



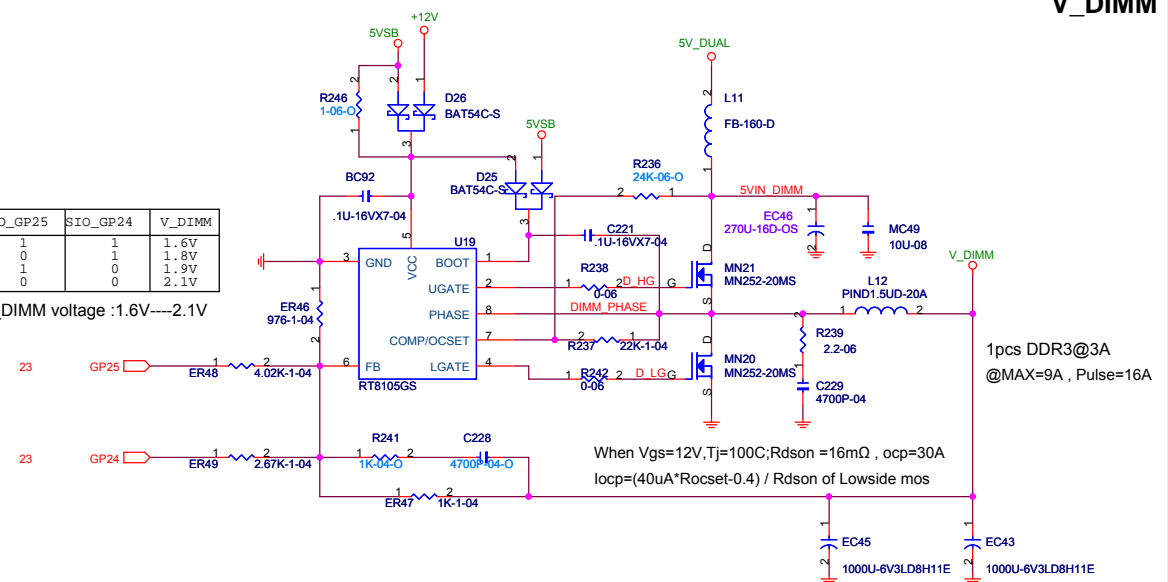
DDRVTT



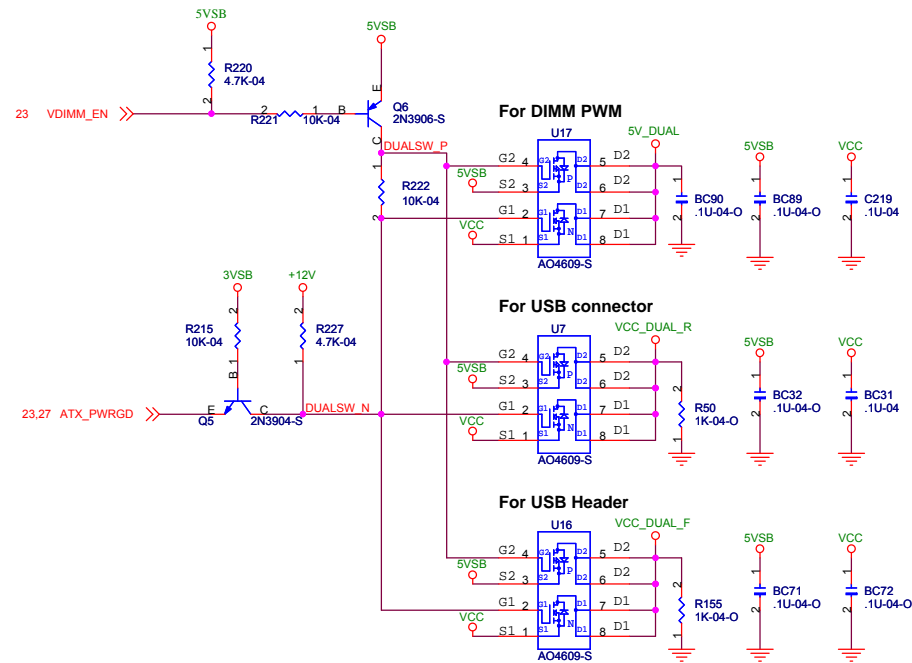
V_DIMM

| SIO_GP25 | SIO_GP24 | V_DIMM |
|----------|----------|--------|
| 1 | 1 | 1.6V |
| 0 | 1 | 1.8V |
| 1 | 0 | 1.9V |
| 0 | 0 | 2.1V |

V_DIMM voltage :1.6V---2.1V



5V_DUAL

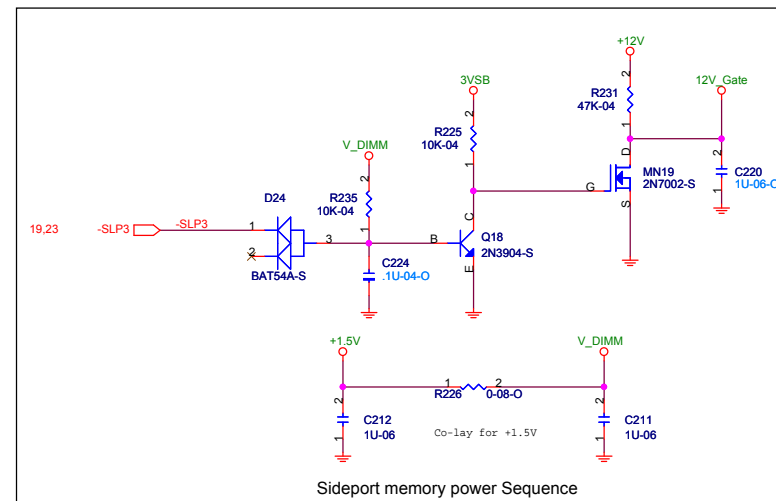
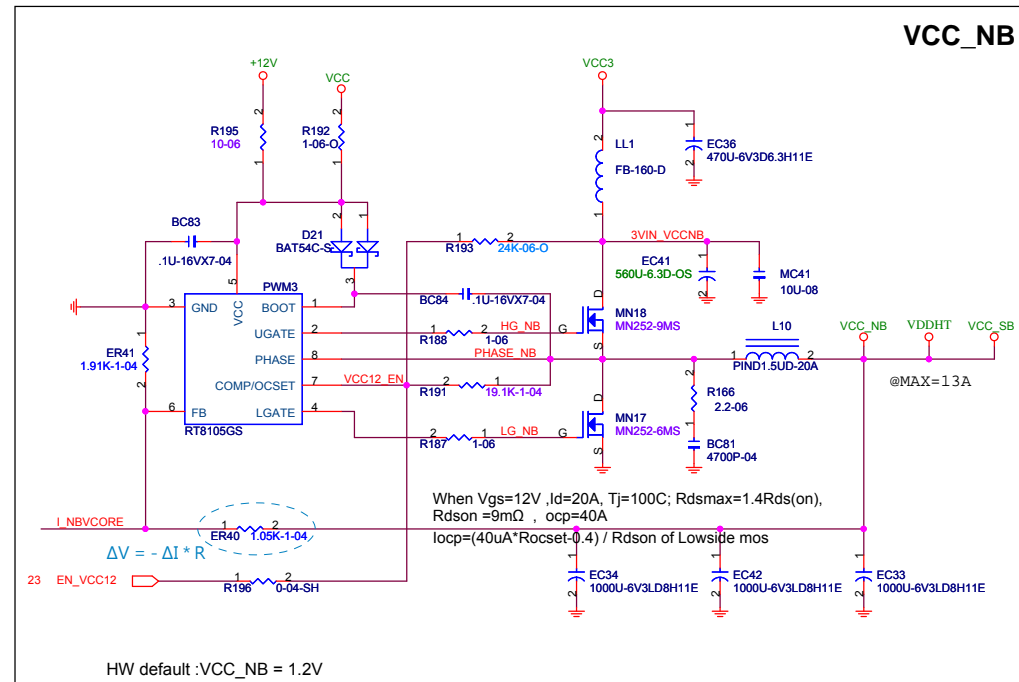
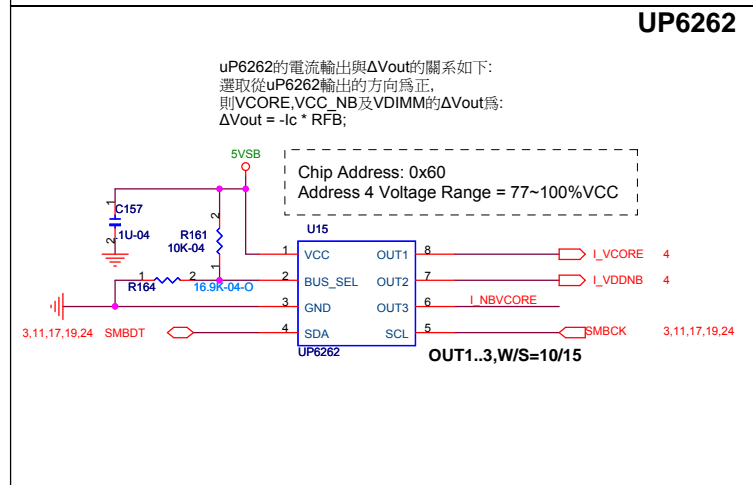
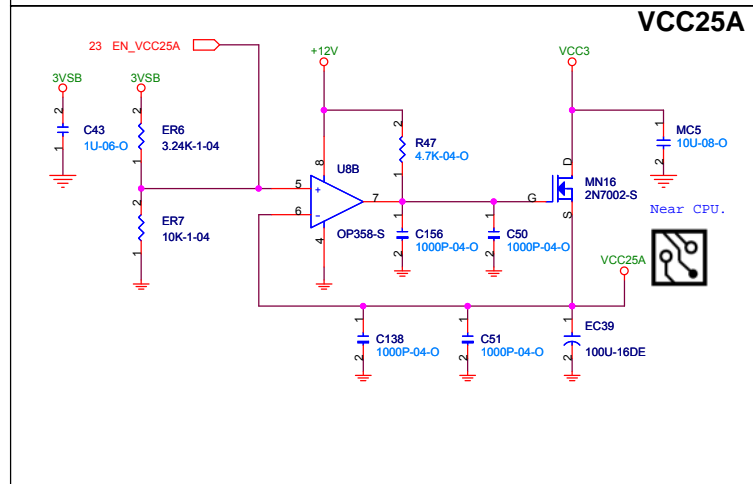
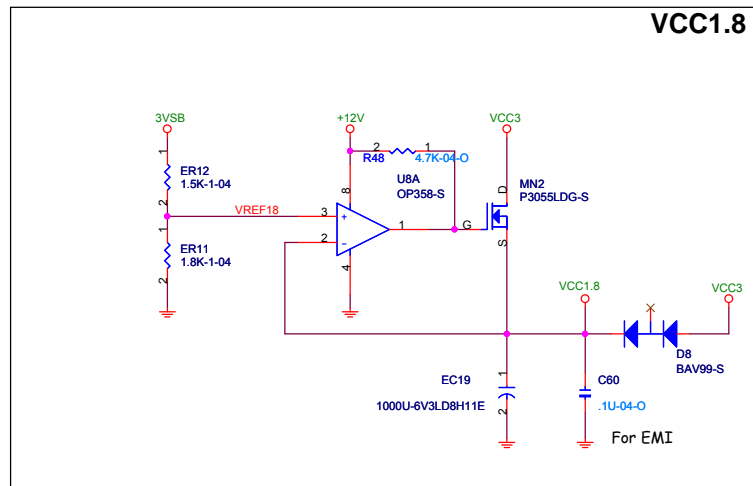


| | S5 | enter S0 | S0 | enter S3 | exit S3 | enter S5 | S5 |
|-----------|------|----------|------|----------|---------|----------|------|
| VDIMM_EN | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| ATX_PWRGD | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| DUALSW_P | 5VSB | 5VSB | 12V | 0 | 12V | 5VSB | 5VSB |
| DUALSW_N | 0 | 12V | 12V | 0 | 12V | 12V | 0 |
| 5V_DUAL | X | VCC5 | VCC5 | 5VSB | VCC5 | VCC5 | 0 |
| VDIMM | X | V | V | V | V | V | X |



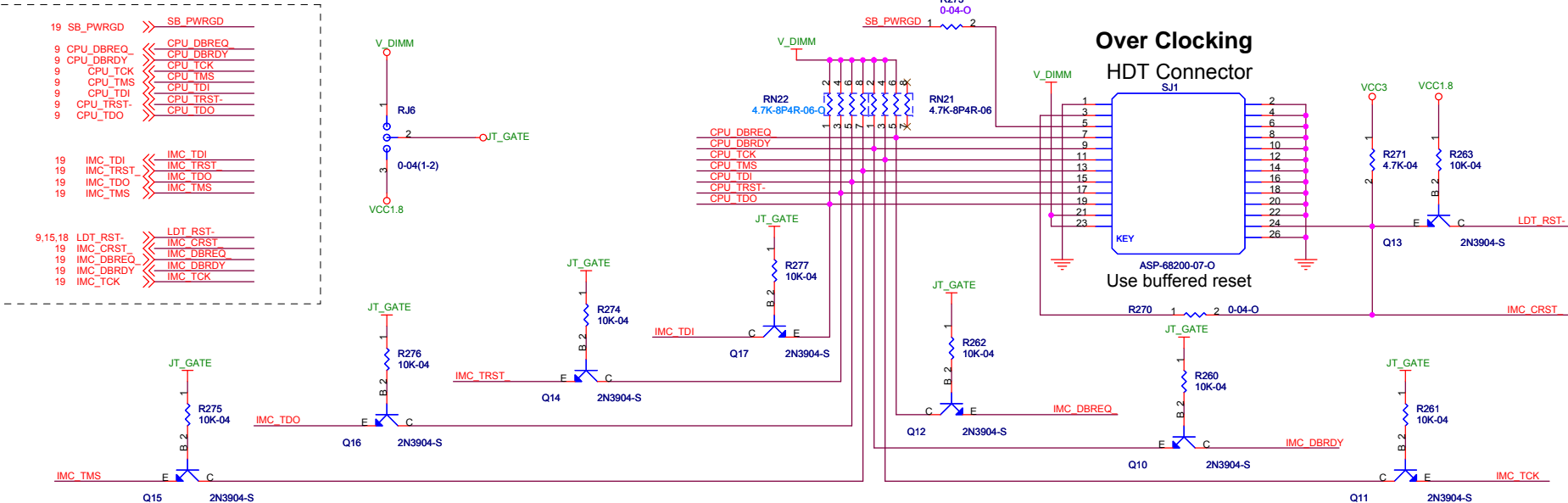
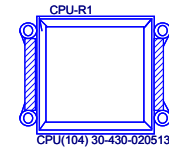
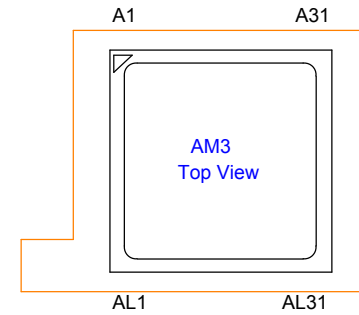
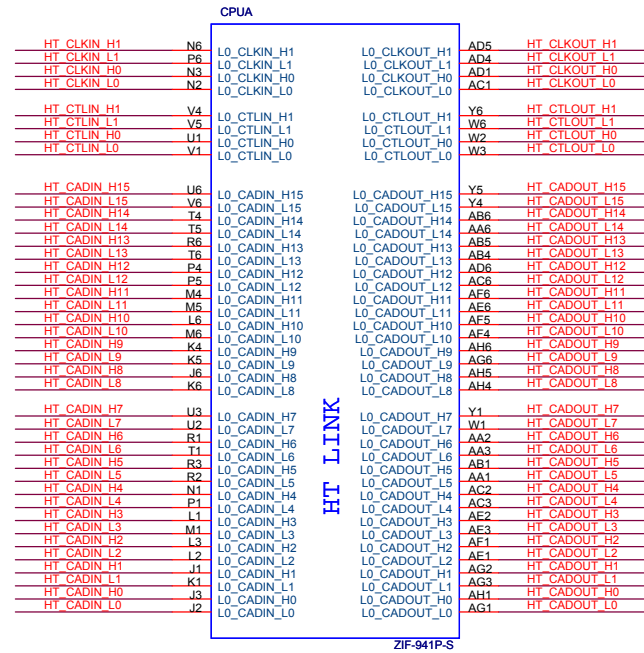
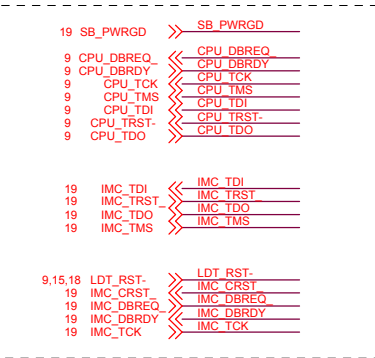
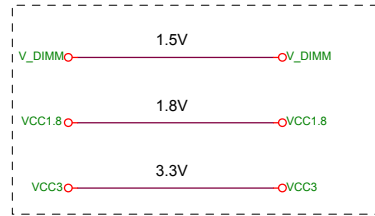
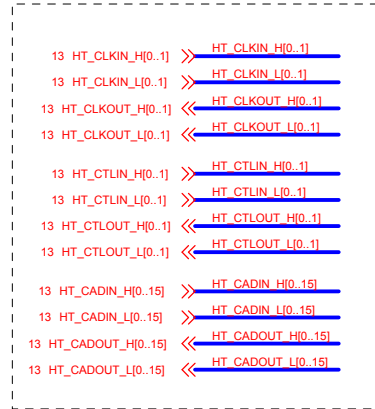
Elitegroup Computer Systems

| Title | |
|-------------------|---------------------------|
| Power A(DC to DC) | |
| Size | Document Number |
| Custom | A885GM-M2 |
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| Rev | 1.0 |



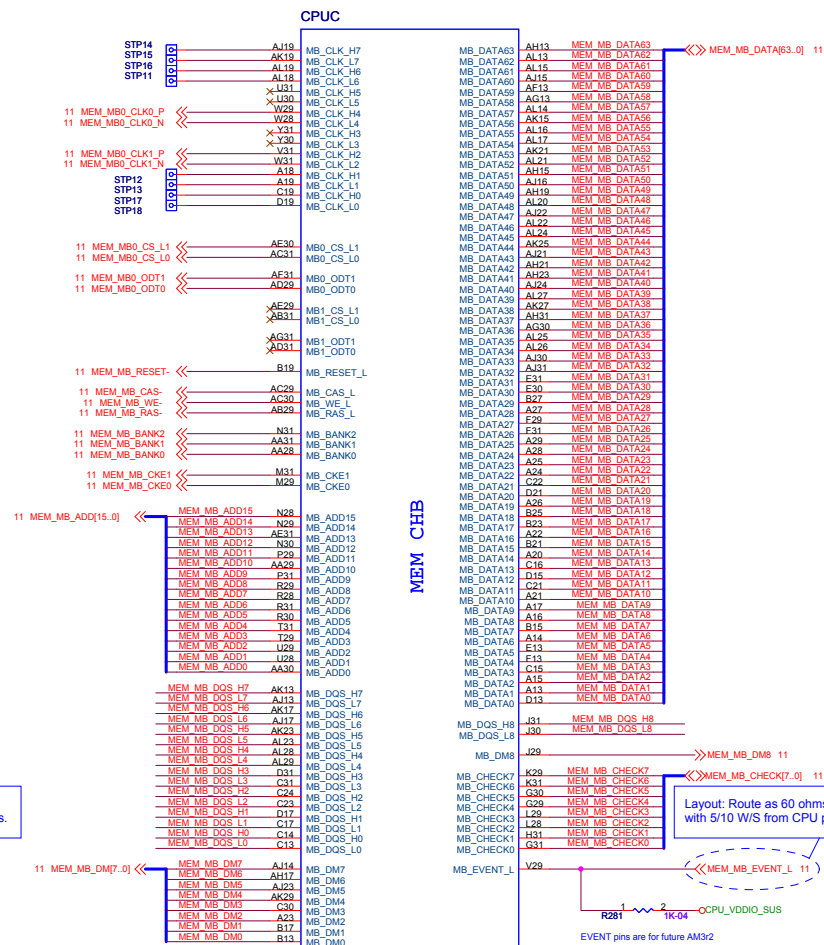
HyperTransport

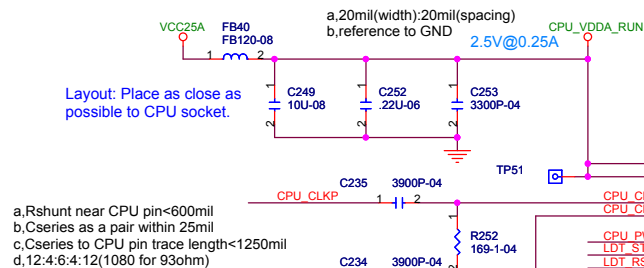
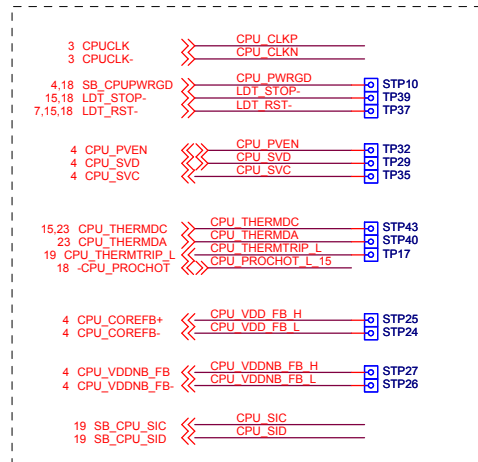
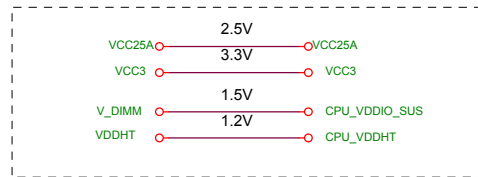
Please use 1mm pad size,
place all ELT test pads
on bottom side only.



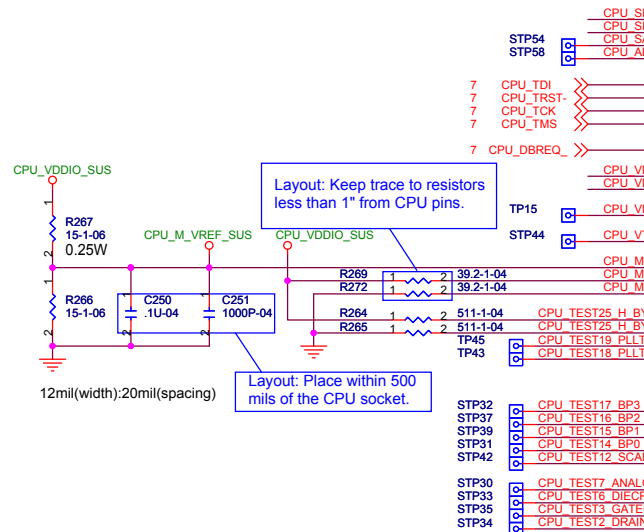


DDR3 Memory Interface B



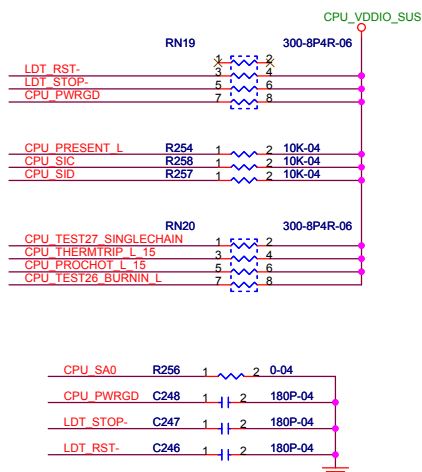


a, Rshunt near CPU pin<600mil
b, Cseries as a pair within 25mil
c, Cseries to CPU pin trace length<1250mil
d, 12:4:6:4:12(1080 for 93ohm)



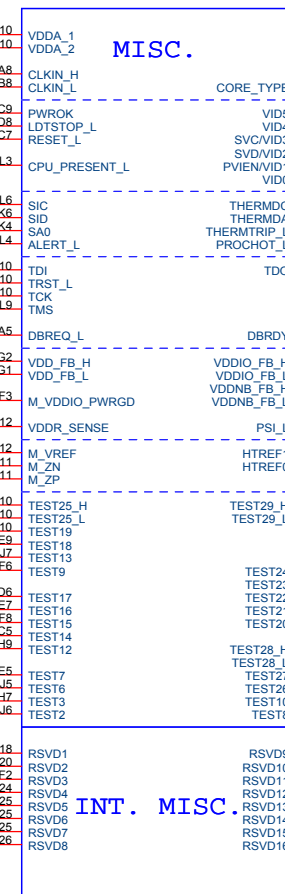
Layout: Keep trace to resistors less than 1" from CPU pins.

Layout: Place within 500 mils of the CPU socket.



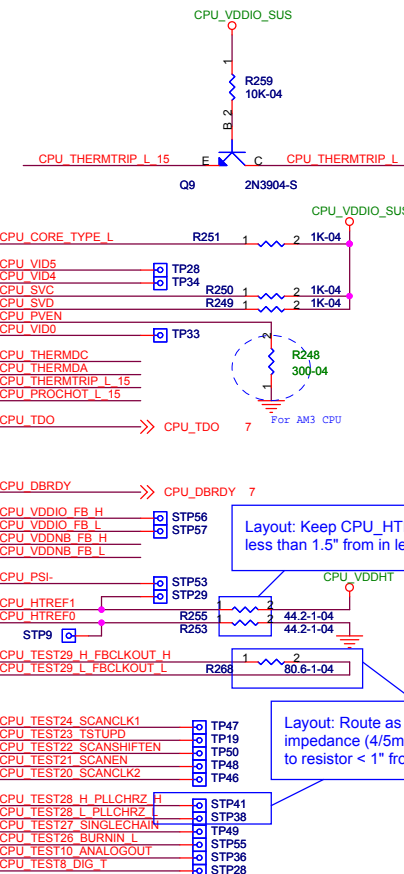
CPU

MISC.



INT. MISC.

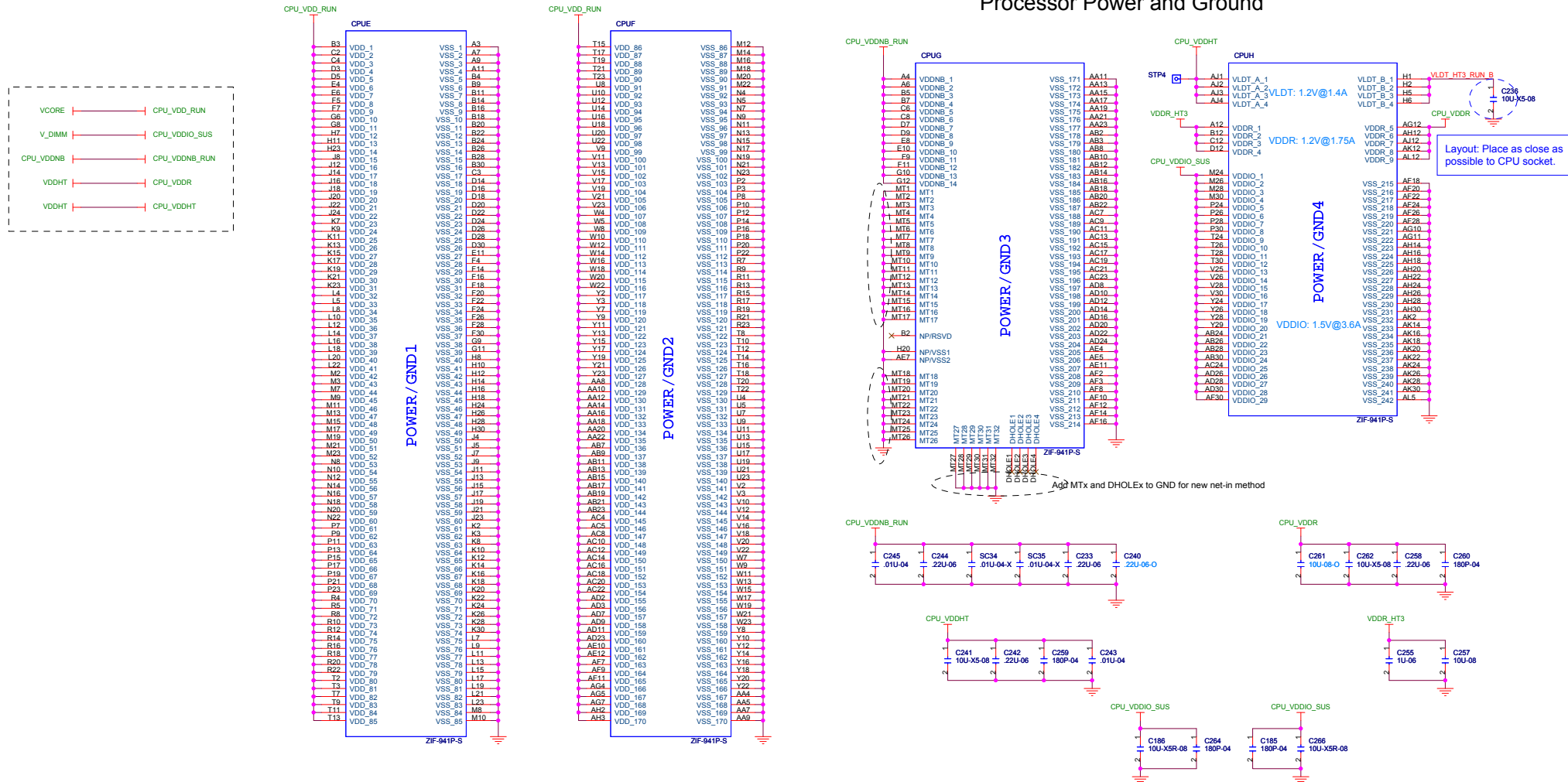
ZIF-941P-S



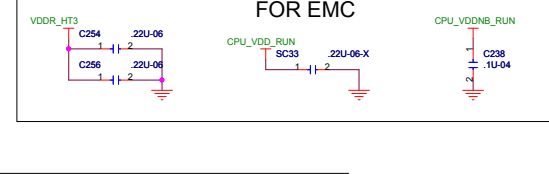
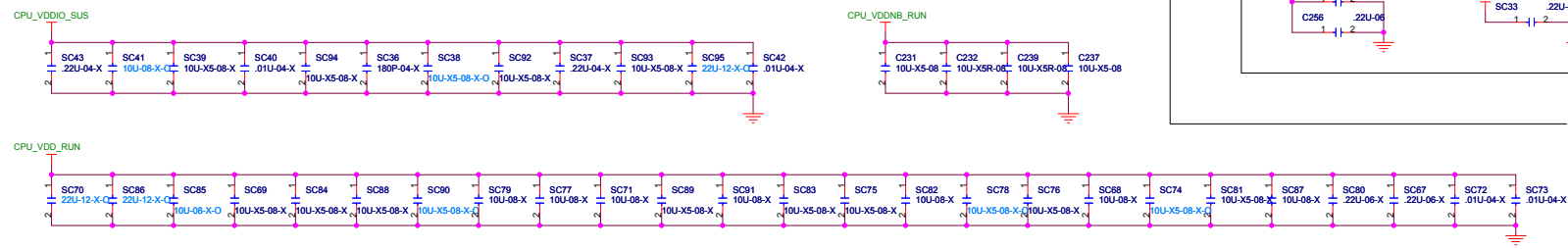
Layout: Keep CPU_HTREF0,1 less than 1.5" from in length.

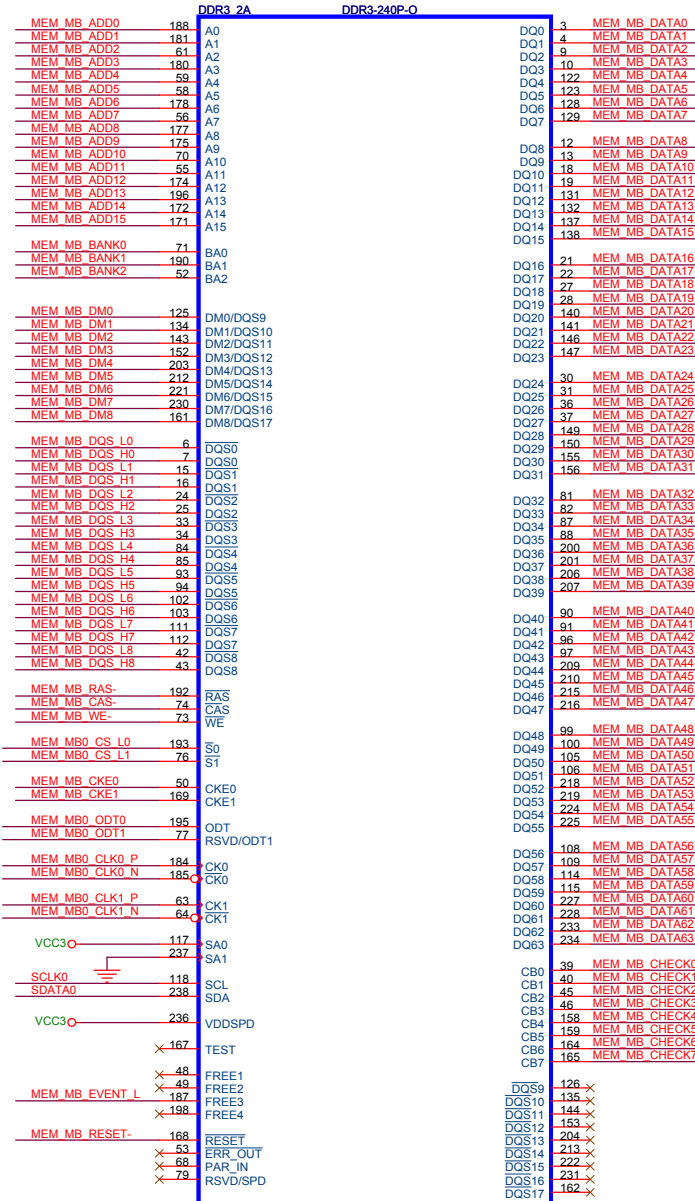
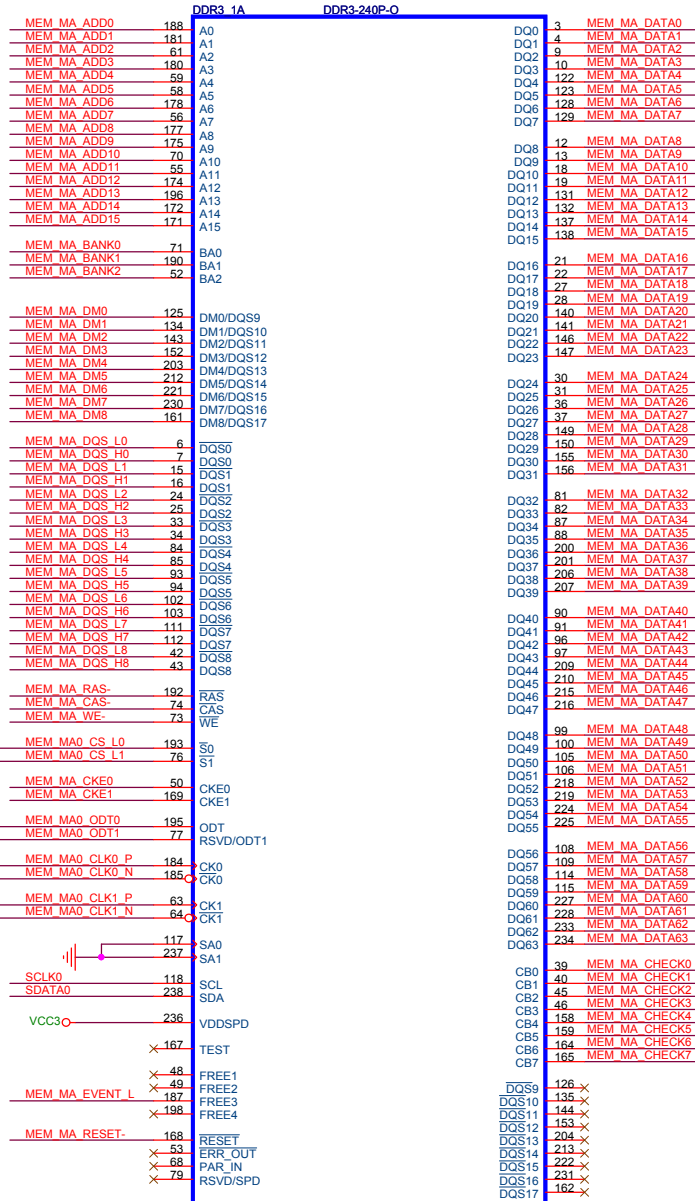
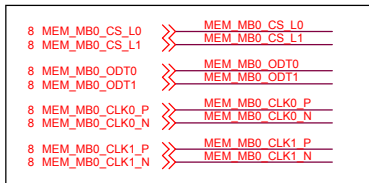
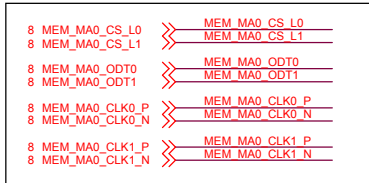
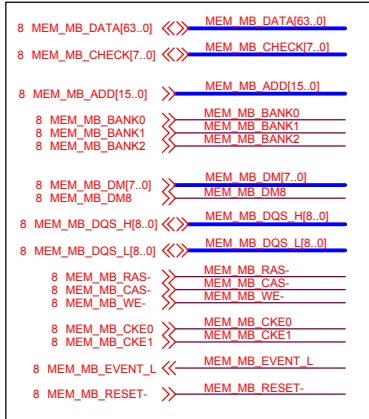
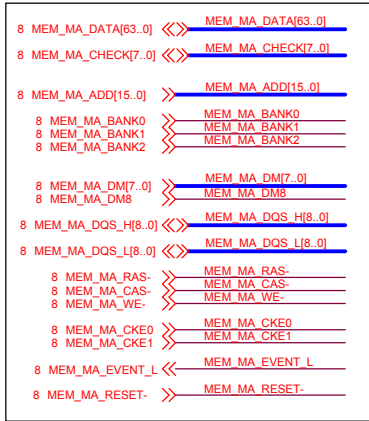
Layout: Route as 80 ohms diff impedance (4/5mil). Keep trace to resistor < 1" from CPU pins.

Processor Power and Ground



Bottom Side Decoupling



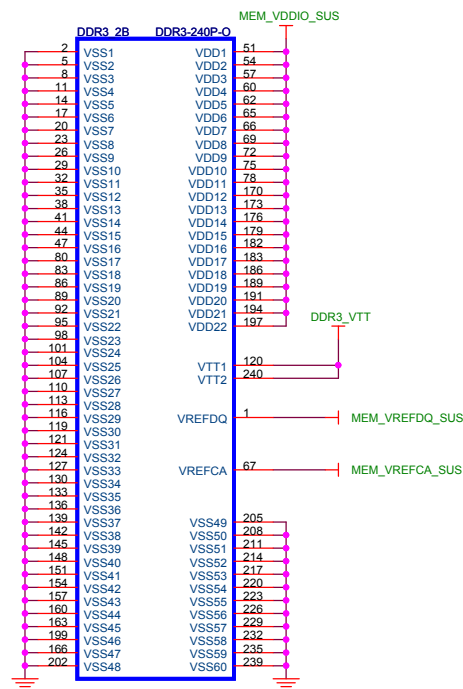
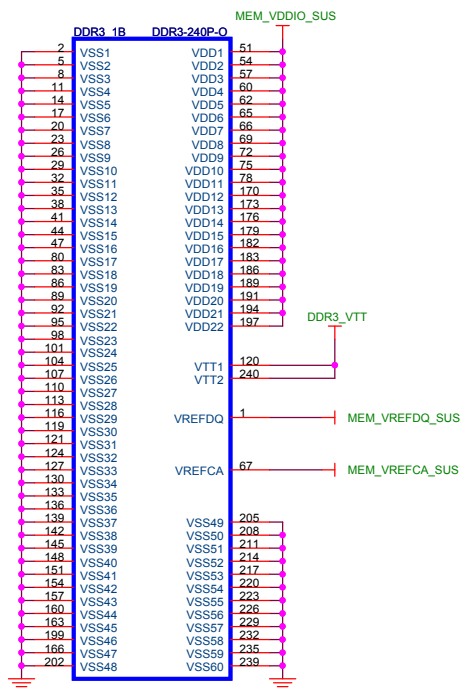
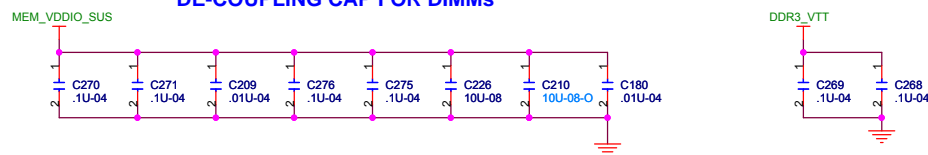


SMBus Addressing

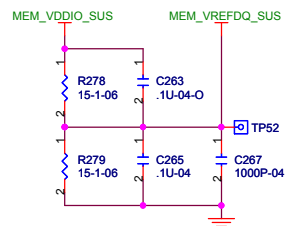
| Device | SMBus 0 |
|--------|---------|
| DIMMA0 | A0 |
| DIMMB0 | A1 |



DE-COUPLING CAP FOR DIMMS

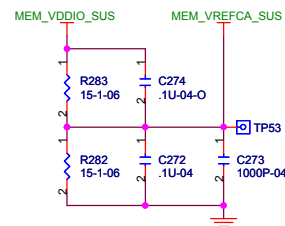


MEM_VREFDQ_SUS



Layout: Place within 500 mils of the DIMMB1 socket.
12mil(width):20mil(spacing)

MEM_VREFCA_SUS

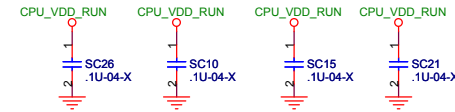


Layout: Place within 500 mils of the DIMMB1 socket.
12mil(width):20mil(spacing)

HT LINK

| | | |
|----------------------|----|--------------------|
| 7 HT_CLKIN_H[0..1] | >> | HT_CLKIN_P[0..1] |
| 7 HT_CLKIN_L[0..1] | >> | HT_CLKIN_N[0..1] |
| 7 HT_CLKOUT_H[0..1] | << | HT_CLKOUT_P[0..1] |
| 7 HT_CLKOUT_L[0..1] | << | HT_CLKOUT_N[0..1] |
| 7 HT_CTLIN_H[0..1] | >> | HT_CTLIN_P[0..1] |
| 7 HT_CTLIN_L[0..1] | >> | HT_CTLIN_N[0..1] |
| 7 HT_CTLOUT_H[0..1] | << | HT_CTLOUT_P[0..1] |
| 7 HT_CTLOUT_L[0..1] | << | HT_CTLOUT_N[0..1] |
| 7 HT_CADIN_H[0..15] | >> | HT_CADIN_P[0..15] |
| 7 HT_CADIN_L[0..15] | >> | HT_CADIN_N[0..15] |
| 7 HT_CADOUT_H[0..15] | << | HT_CADOUT_P[0..15] |
| 7 HT_CADOUT_L[0..15] | << | HT_CADOUT_N[0..15] |

TX signals return path CAP , Placed near the North Bridge



NBA

PART 1 OF 6

HYPER TRANSPORT CPU I/F

| | | | | |
|---------------|------|-------------|-----|--------------|
| HT_CADOUT_P0 | Y25 | HT_RXCAD0P | D24 | HT_CADIN_P0 |
| HT_CADOUT_N0 | Y24 | HT_RXCAD0N | D25 | HT_CADIN_N0 |
| HT_CADOUT_P1 | V22 | HT_RXCAD1P | E24 | HT_CADIN_P1 |
| HT_CADOUT_N1 | V23 | HT_RXCAD1N | E25 | HT_CADIN_N1 |
| HT_CADOUT_P2 | V25 | HT_RXCAD2P | E24 | HT_CADIN_P2 |
| HT_CADOUT_N2 | V24 | HT_RXCAD2N | E25 | HT_CADIN_N2 |
| HT_CADOUT_P3 | U24 | HT_RXCAD3P | E23 | HT_CADIN_P3 |
| HT_CADOUT_N3 | U25 | HT_RXCAD3N | E24 | HT_CADIN_N3 |
| HT_CADOUT_P4 | T24 | HT_RXCAD4P | E23 | HT_CADIN_P4 |
| HT_CADOUT_N4 | T25 | HT_RXCAD4N | E24 | HT_CADIN_N4 |
| HT_CADOUT_P5 | P22 | HT_RXCAD5P | E23 | HT_CADIN_P5 |
| HT_CADOUT_N5 | P23 | HT_RXCAD5N | E24 | HT_CADIN_N5 |
| HT_CADOUT_P6 | P25 | HT_RXCAD6P | K24 | HT_CADIN_P6 |
| HT_CADOUT_N6 | P24 | HT_RXCAD6N | K25 | HT_CADIN_N6 |
| HT_CADOUT_P7 | N24 | HT_RXCAD7P | K23 | HT_CADIN_P7 |
| HT_CADOUT_N7 | N25 | HT_RXCAD7N | K22 | HT_CADIN_N7 |
| HT_CADOUT_P8 | AC24 | HT_RXCAD8P | F21 | HT_CADIN_P8 |
| HT_CADOUT_N8 | AC25 | HT_RXCAD8N | G21 | HT_CADIN_N8 |
| HT_CADOUT_P9 | AB25 | HT_RXCAD9P | G20 | HT_CADIN_P9 |
| HT_CADOUT_N9 | AB24 | HT_RXCAD9N | J21 | HT_CADIN_N9 |
| HT_CADOUT_P10 | AA24 | HT_RXCAD10P | J20 | HT_CADIN_P10 |
| HT_CADOUT_N10 | AA25 | HT_RXCAD10N | J21 | HT_CADIN_N10 |
| HT_CADOUT_P11 | Y22 | HT_RXCAD11P | J18 | HT_CADIN_P11 |
| HT_CADOUT_N11 | Y23 | HT_RXCAD11N | K17 | HT_CADIN_N11 |
| HT_CADOUT_P12 | W21 | HT_RXCAD12P | L19 | HT_CADIN_P12 |
| HT_CADOUT_N12 | W20 | HT_RXCAD12N | J19 | HT_CADIN_N12 |
| HT_CADOUT_P13 | V21 | HT_RXCAD13P | M19 | HT_CADIN_P13 |
| HT_CADOUT_N13 | V20 | HT_RXCAD13N | L18 | HT_CADIN_N13 |
| HT_CADOUT_P14 | U20 | HT_RXCAD14P | M21 | HT_CADIN_P14 |
| HT_CADOUT_N14 | U21 | HT_RXCAD14N | P21 | HT_CADIN_N14 |
| HT_CADOUT_P15 | U19 | HT_RXCAD15P | P18 | HT_CADIN_P15 |
| HT_CADOUT_N15 | U18 | HT_RXCAD15N | M18 | HT_CADIN_N15 |
| HT_CLKOUT_P0 | T22 | HT_RXCLK0P | H24 | HT_CLKIN_P0 |
| HT_CLKOUT_N0 | T23 | HT_RXCLK0N | H25 | HT_CLKIN_N0 |
| HT_CLKOUT_P1 | AB23 | HT_RXCLK1P | L21 | HT_CLKIN_P1 |
| HT_CLKOUT_N1 | AA22 | HT_RXCLK1N | L20 | HT_CLKIN_N1 |
| HT_CTLOUT_P0 | M22 | HT_RXCTL0P | M24 | HT_CTLIN_P0 |
| HT_CTLOUT_N0 | M23 | HT_RXCTL0N | M25 | HT_CTLIN_N0 |
| HT_CTLOUT_P1 | R21 | HT_RXCTL1P | P19 | HT_CTLIN_P1 |
| HT_CTLOUT_N1 | R20 | HT_RXCTL1N | R18 | HT_CTLIN_N1 |
| HT_RXCALP | C23 | HT_RXCALP | B24 | HT_TXCALP |
| HT_RXCALN | A24 | HT_RXCALN | B25 | HT_TXCALN |

RS880P-A11
01-201-880180

PCI-E 16X

PCI-E lan

NBB

PART 2 OF 6

PCI-E I/F GPP

PCI-E I/F GPP

PCI-E I/F SB

PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

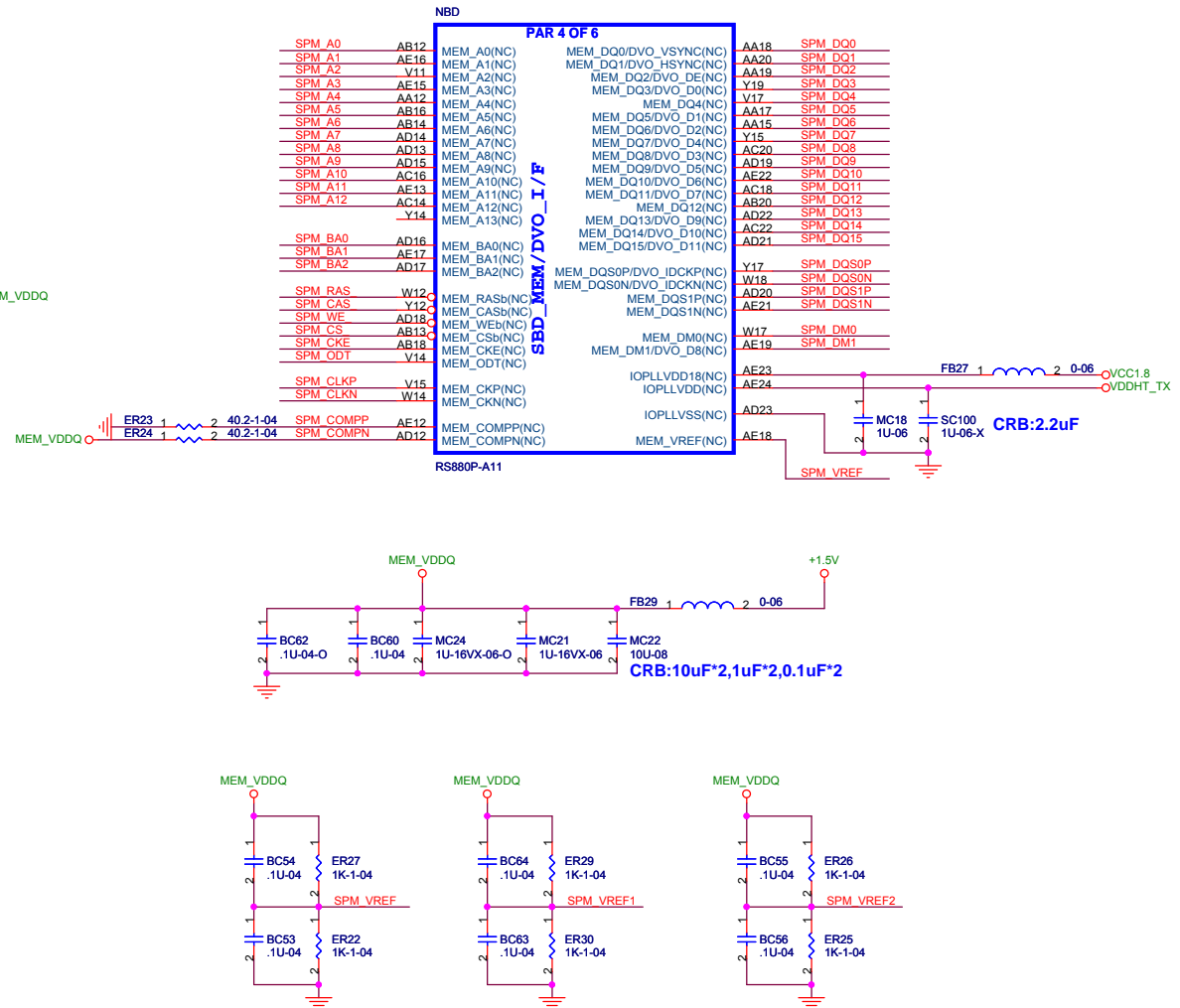
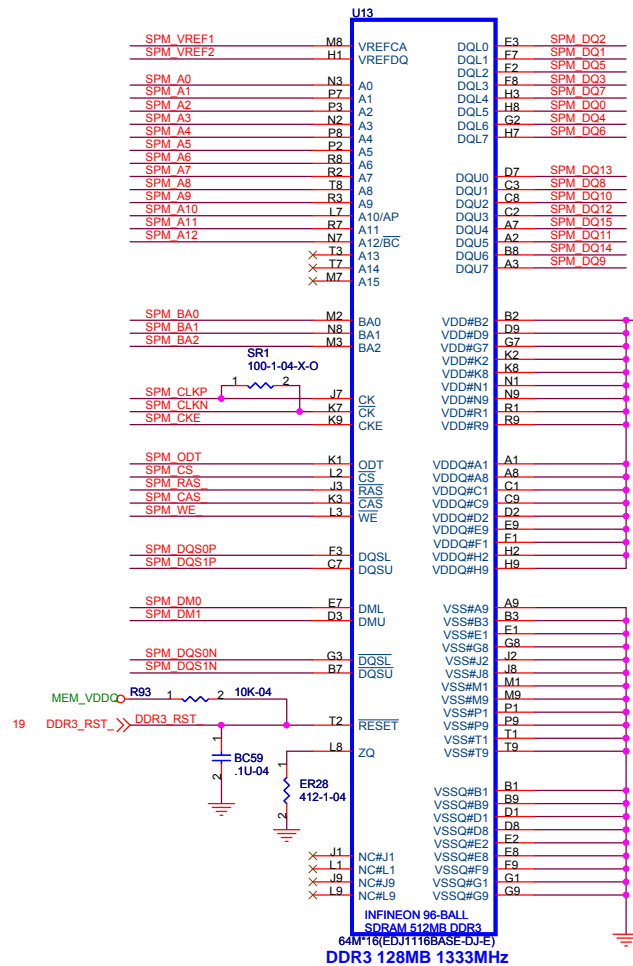
RS880P-A11

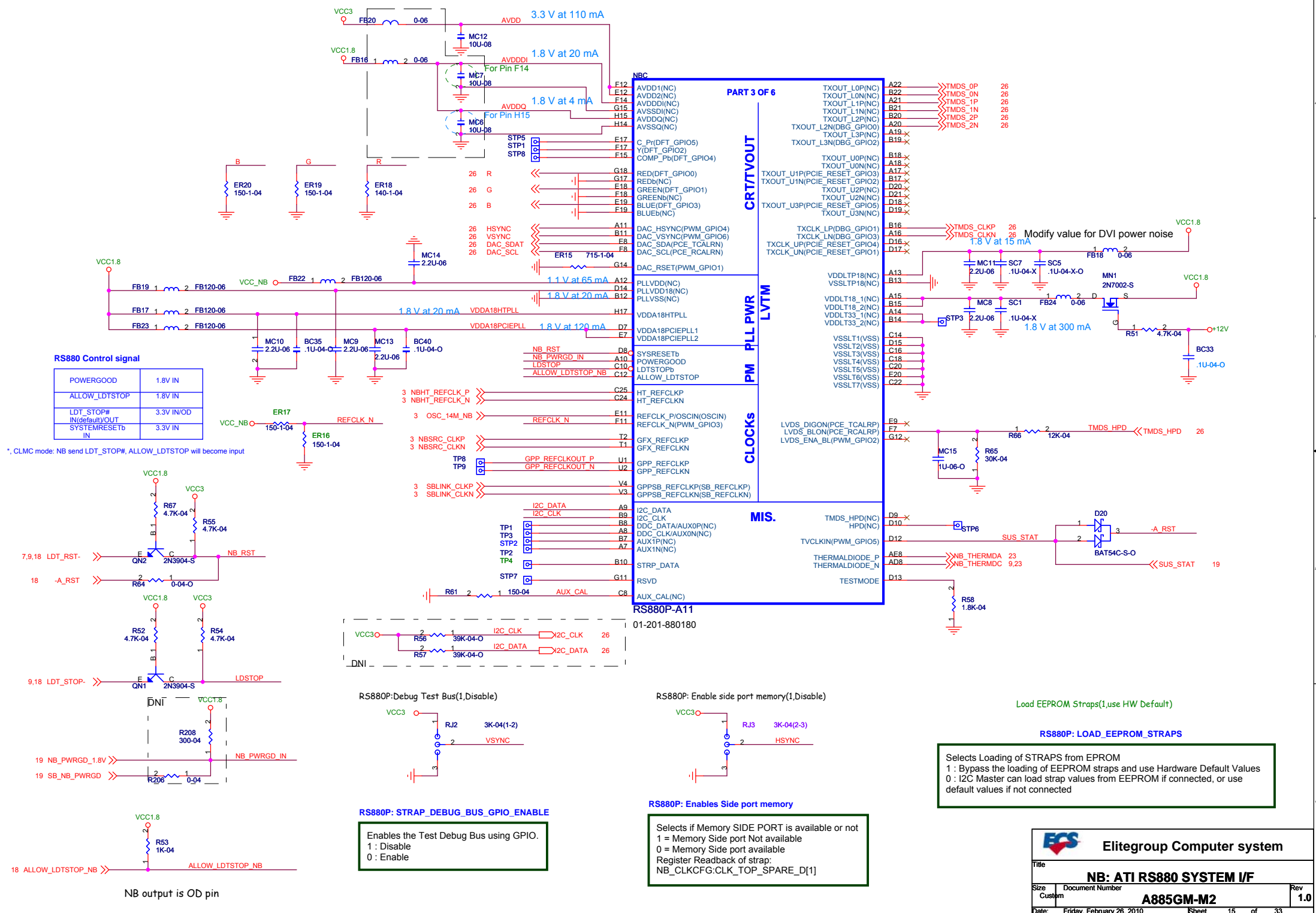
01-201-880180



Elitegroup Computer system

| | | | |
|----------|---------------------------|-----------|----------|
| File | NB:ATI RS880 LINK I/F | | |
| Size | Document Number | A885GM-M2 | |
| Customer | | Rev 1.0 | |
| Date | Friday, February 26, 2010 | Sheet | 13 of 33 |

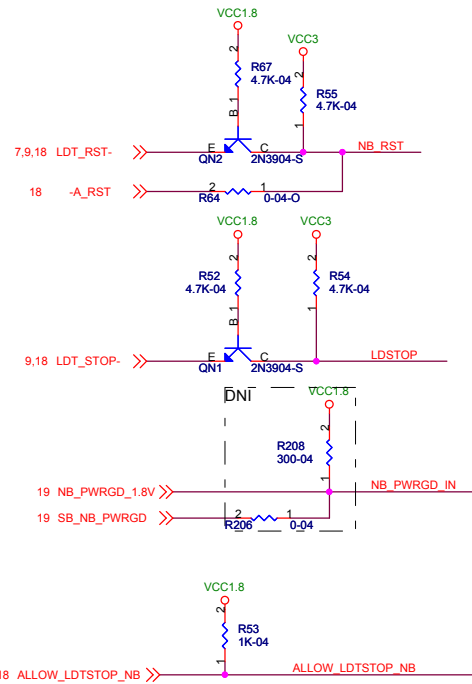




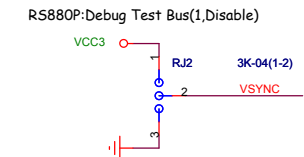
RS880 Control signal

| | |
|-----------------|------------|
| POWERGOOD | 1.8V IN |
| ALLOW_LDTSTOP | 1.8V IN |
| LDT_STOP# | 3.3V IN/OD |
| IN(default)/OUT | |
| SYSTEMRESETb | 3.3V IN |
| IN | |

*, CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input

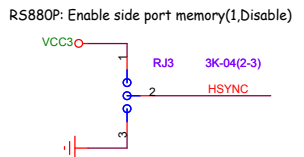


NB output is OD pin



RS880P: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO.
1 : Disable
0 : Enable



RS880P: Enables Side port memory

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap:
NB_CLKCFG:CLK_TOP_SPARE_D[1]

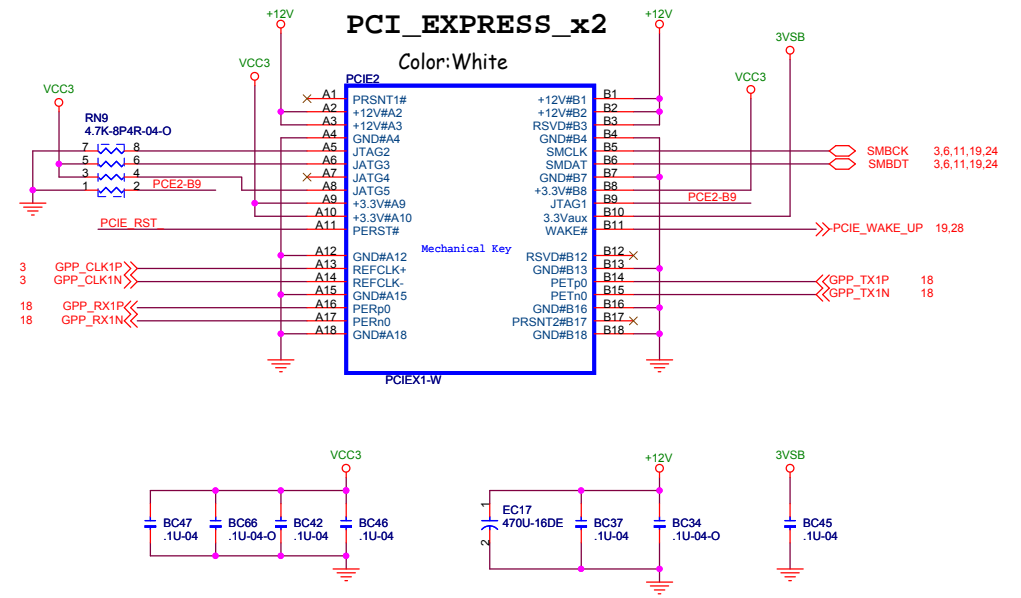
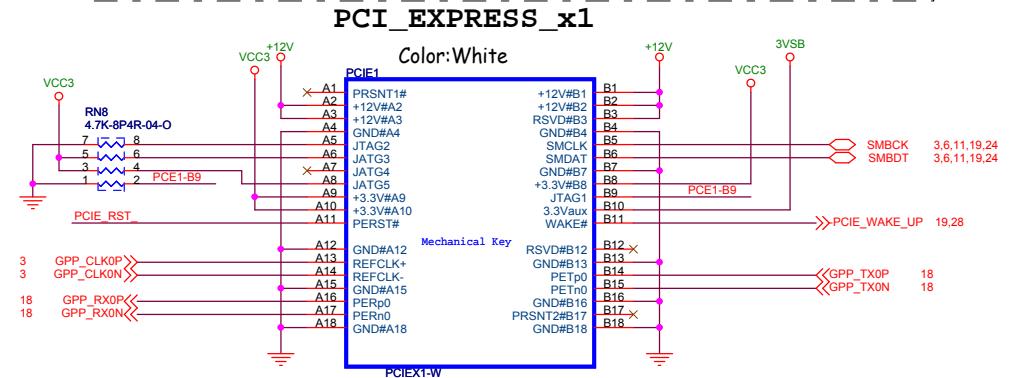
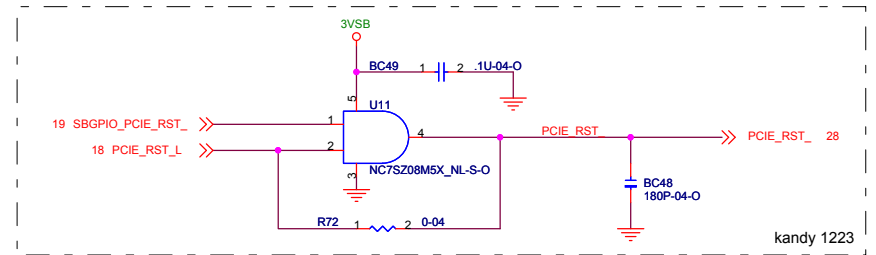
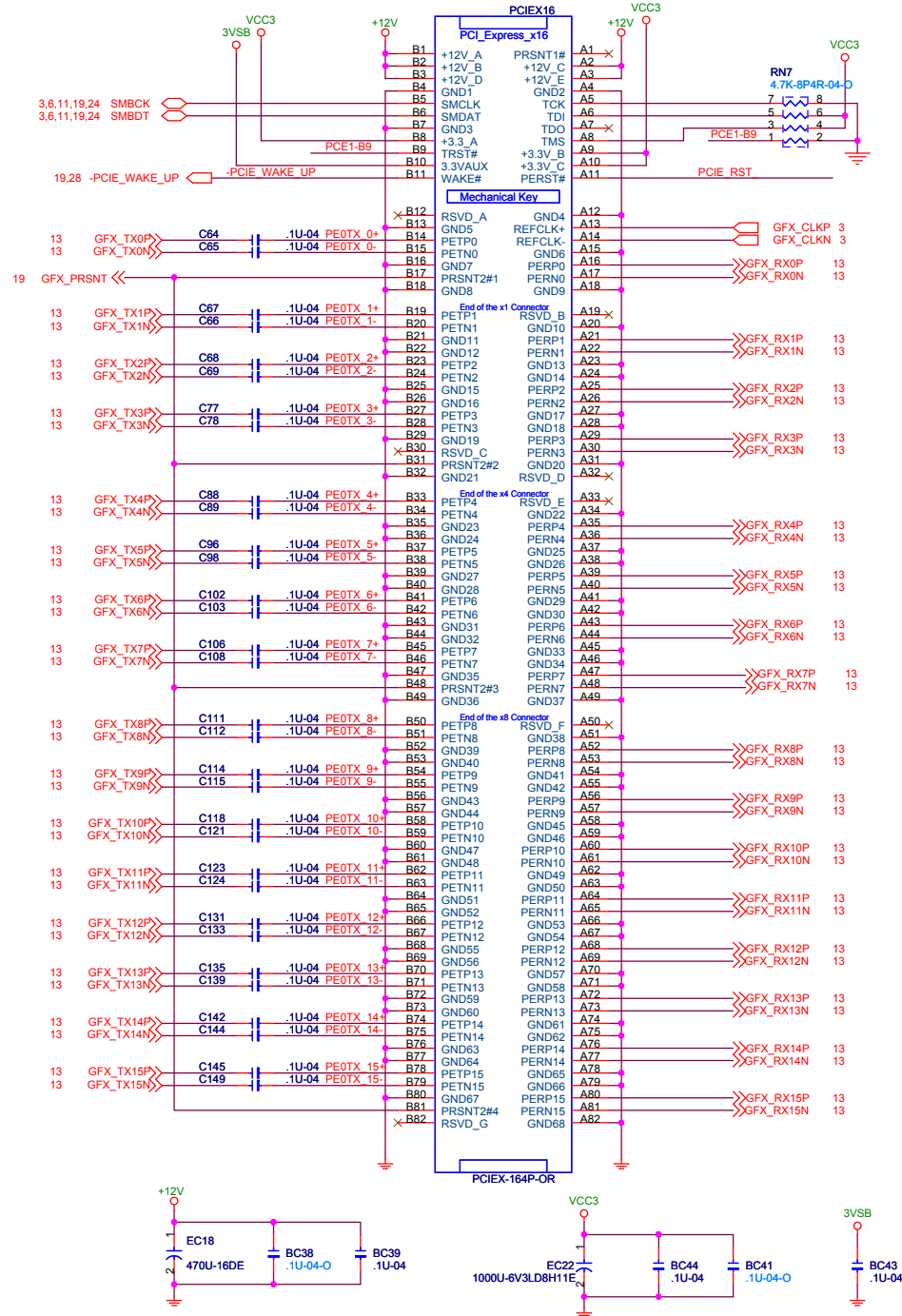
Load EEPROM Straps(1,use HW Default)

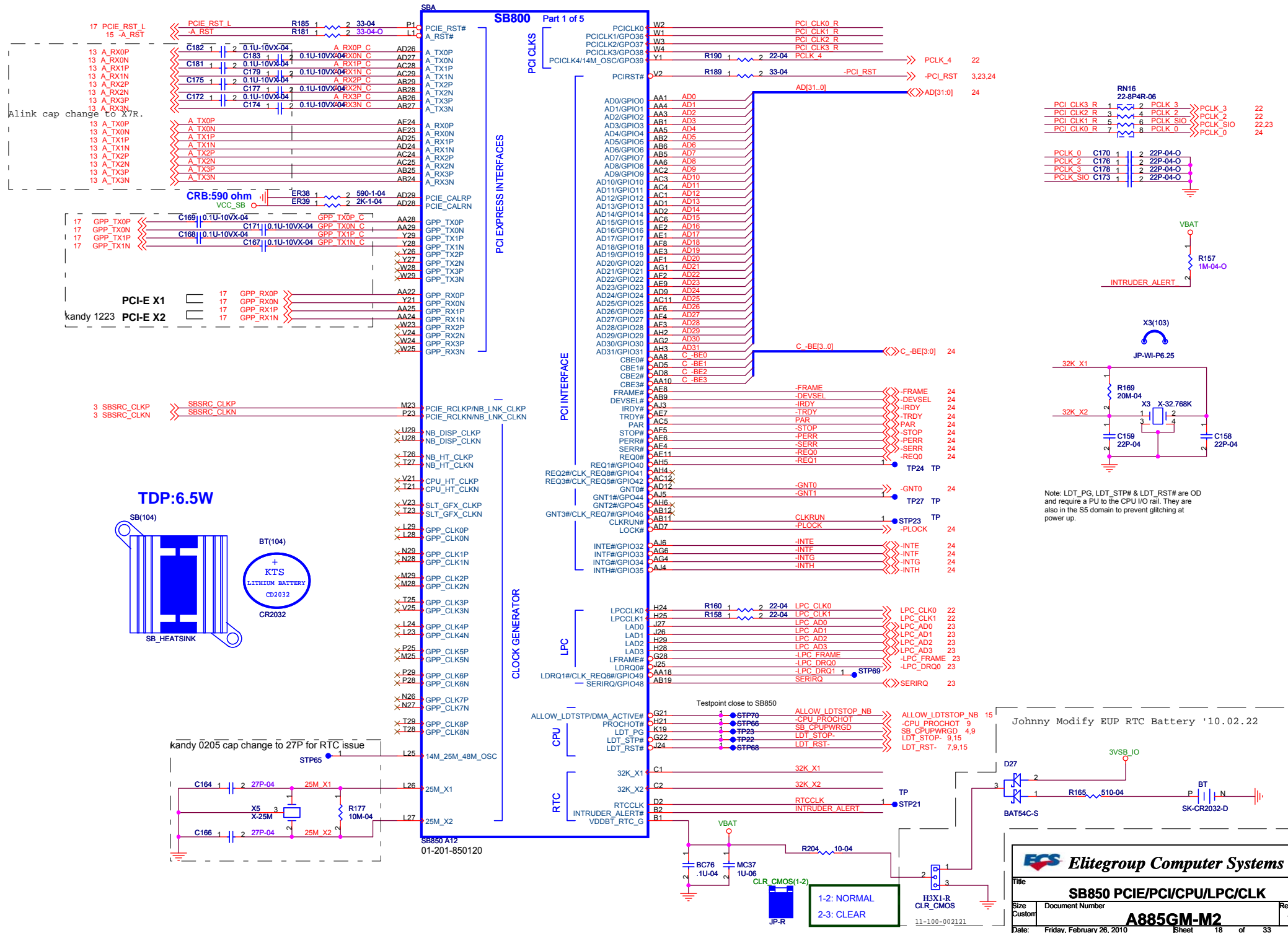
RS880P: LOAD_EEPROM_STRAPS

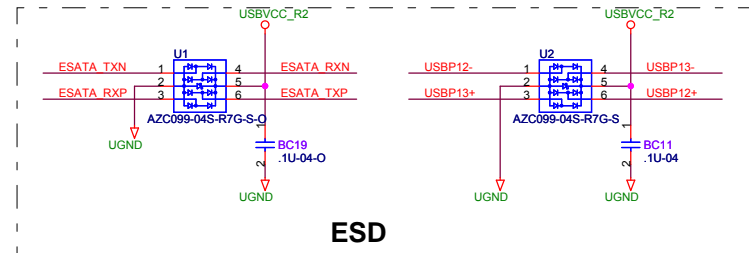
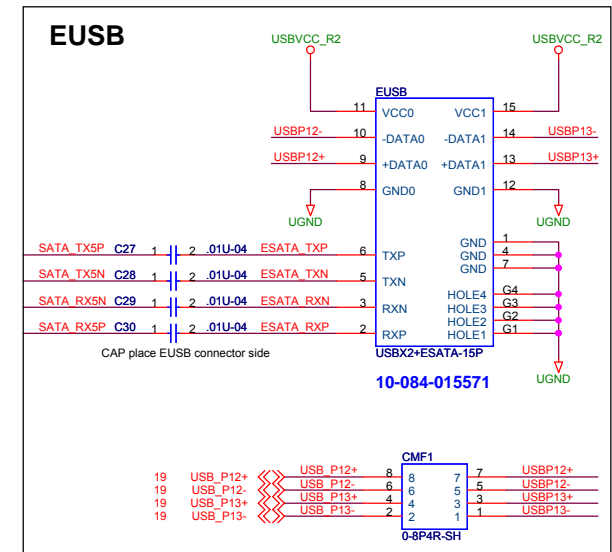
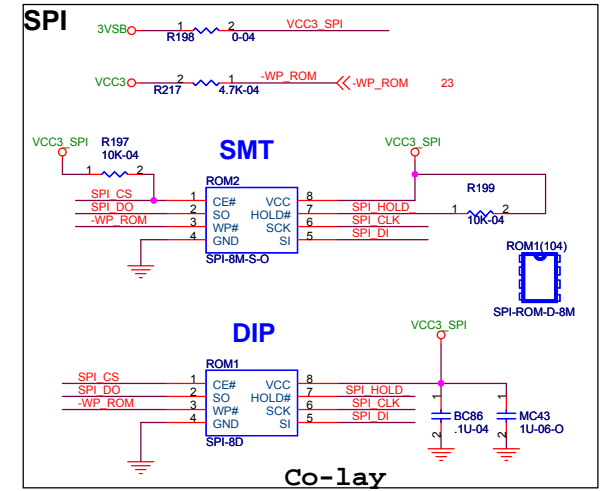
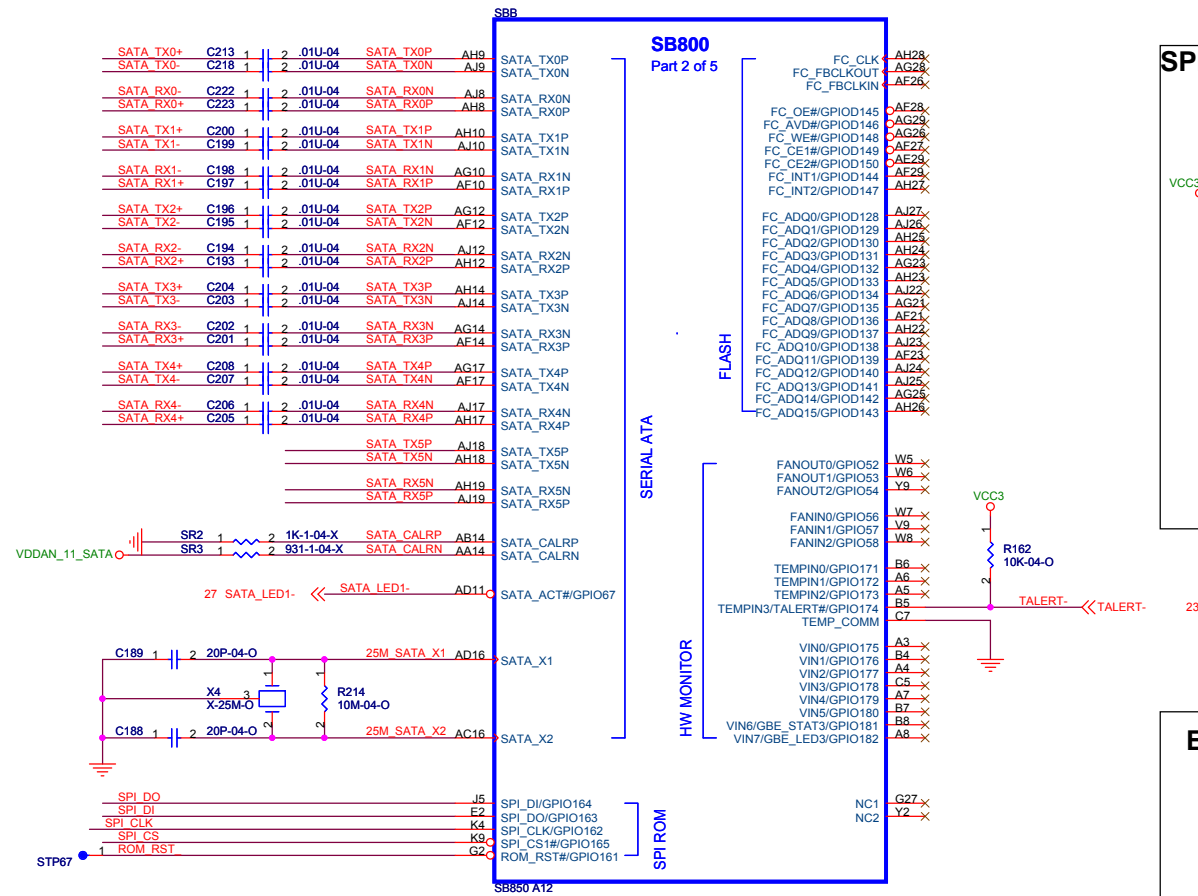
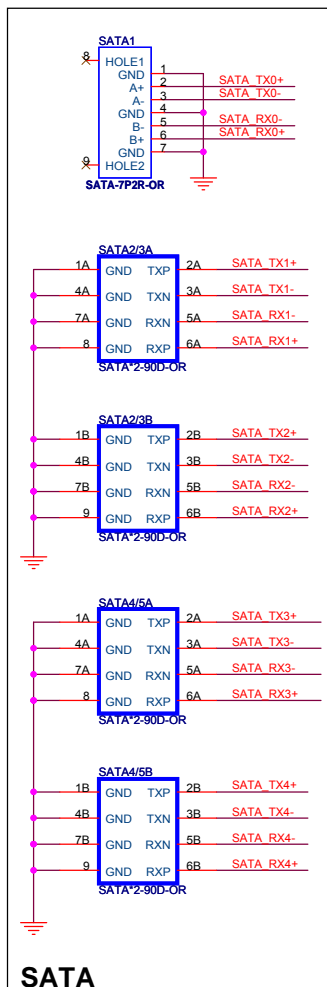
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

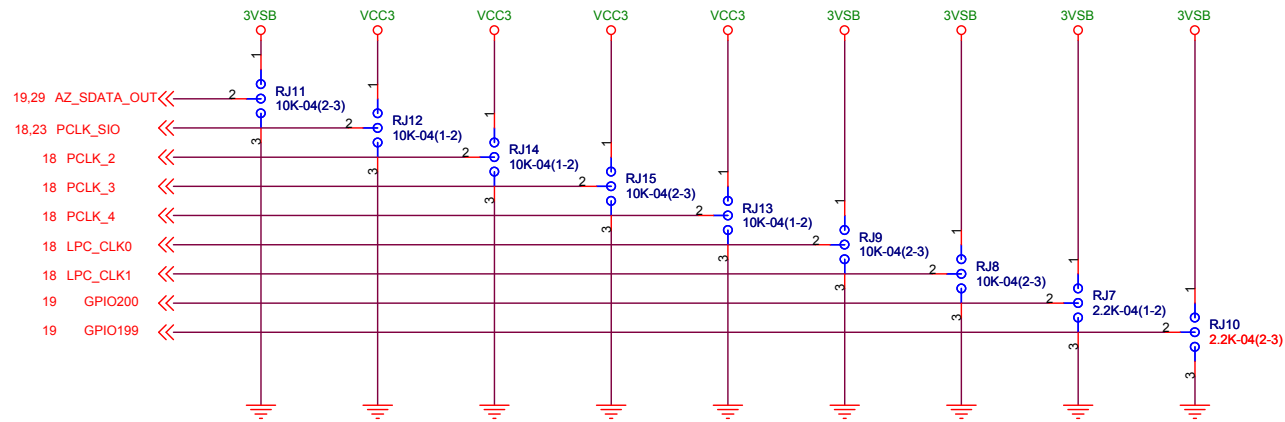
PCI_EXPRESS_x16

Color:Orange +12V:5.5Amp







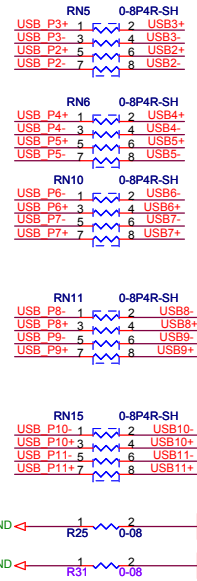
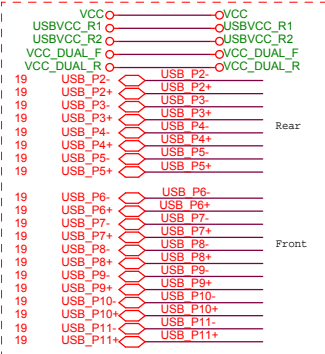


REQUIRED STRAPS

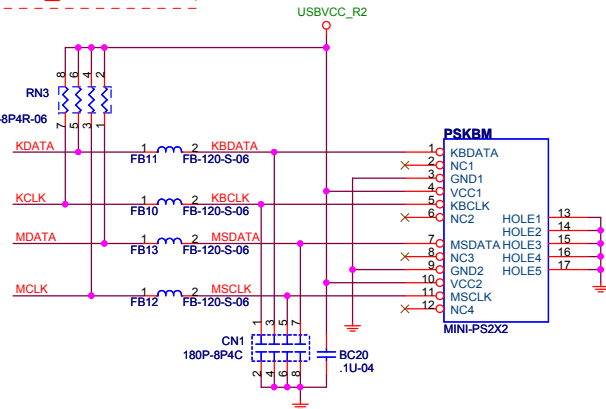
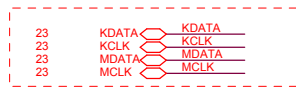
| | AZ_SDOUT | PCI_CLK1 | PCI_CLK2 | PCI_CLK3 | PCI_CLK4 | LPC_CLK0 | LPC_CLK1 | GP200 | GP199 |
|-----------|-----------------------------|----------------------------|-----------------------------------|-------------------------------|----------------------------------|------------------------|----------------------------|---|----------------------------------|
| PULL HIGH | LOW POWER MODE | ALLOW PCIE GEN2 DEFAULT | Watchdog Timer Enabled DEFAULT | USE DEBUG STRAP | Non Fusion CLOCK MODE DEFAULT | EC ENABLED | CLKGEN ENABLED | ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT | |
| PULL LOW | PERFORMANCE MODE DEFAULT | FORCE PCIE GEN1 | Watchdog Timer Disabled | IGNORE DEBUG STRAP DEFAULT | Fusion CLOCK MODE | EC DISABLED DEFAULT | CLKGEN DISABLED DEFAULT | | L, H = LPC ROM L, L = FWH ROM |

DELETE IDE

External Connection



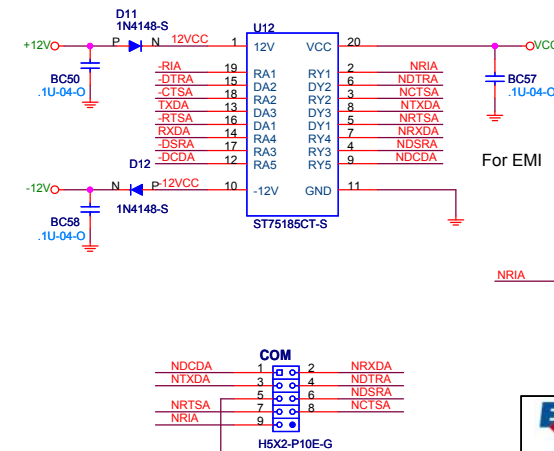
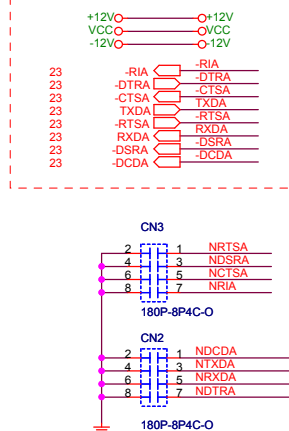
External Connection



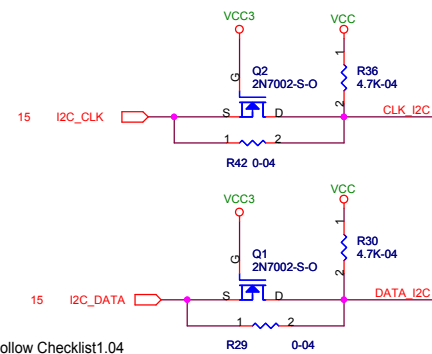
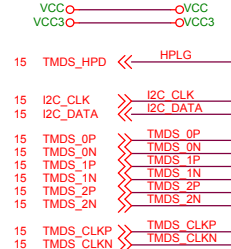
PSKBM

COM Header

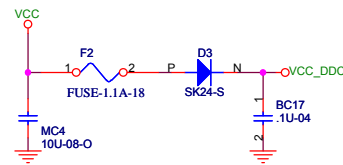
External Connection



External Connection



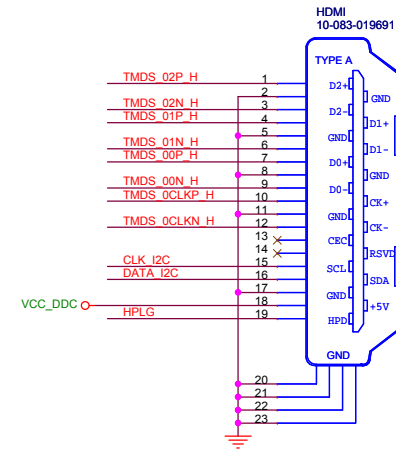
Follow Checklist1.04 R29 0-04
Pulled up to +5.0 V with a 4.7k 5% resistor; Level shifter not required.



HDMI

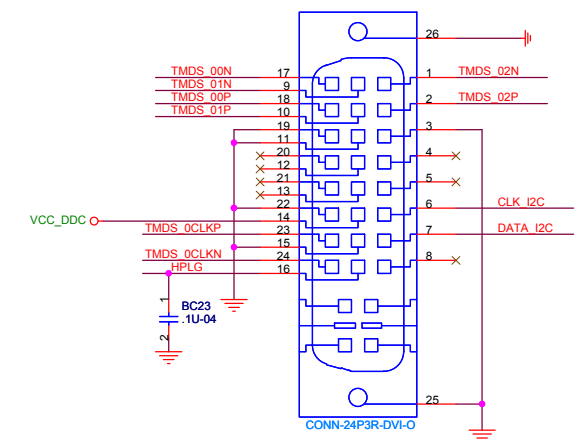
| SRN1 | | CMK-90-1206-X | |
|-----------|---|---------------|----------------|
| TMDS_CLKN | 1 | 2 | 2 TMDS_0CLKN H |
| TMDS_CLKP | 3 | 4 | 4 TMDS_0CLKP H |
| TMDS_0P | 5 | 6 | 6 TMDS_00P H |
| TMDS_0N | 7 | 8 | 8 TMDS_00N H |

| SRN2 | | CMK-90-1206-X | |
|---------|---|---------------|--------------|
| TMDS_1P | 1 | 2 | 2 TMDS_01P H |
| TMDS_1N | 3 | 4 | 4 TMDS_01N H |
| TMDS_2P | 5 | 6 | 6 TMDS_02P H |
| TMDS_2N | 7 | 8 | 8 TMDS_02N H |

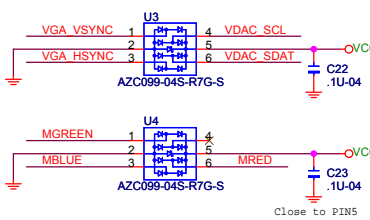
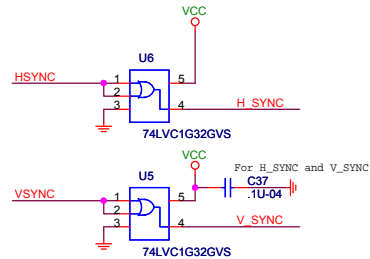
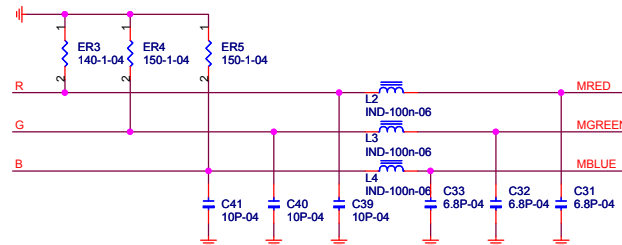
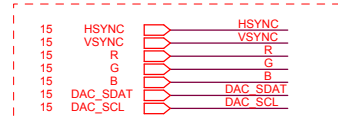


DVI

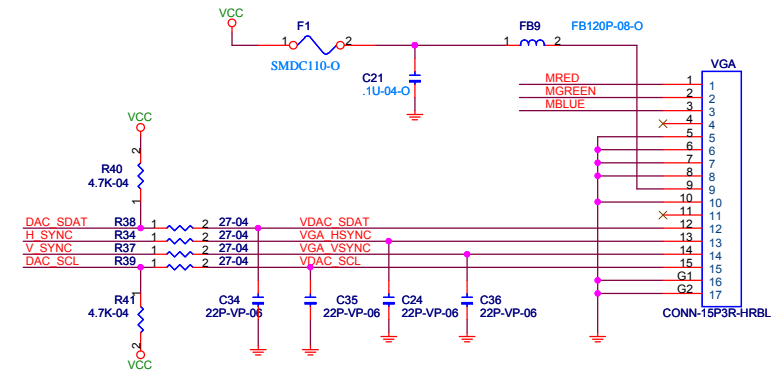
| Header | Pin | Signal |
|--------|-----|------------|
| RN1 | 1 | TMD5_2N |
| RN1 | 2 | TMD5_2P |
| RN1 | 3 | TMD5_1N |
| RN1 | 4 | TMD5_1P |
| RN1 | 5 | TMD5_0N |
| RN1 | 6 | TMD5_0P |
| RN1 | 7 | TMD5_0CLKP |
| RN1 | 8 | TMD5_0CLKN |
| RN2 | 1 | TMD5_0N |
| RN2 | 2 | TMD5_0P |
| RN2 | 3 | TMD5_0CLKP |
| RN2 | 4 | TMD5_0CLKN |
| RN2 | 5 | TMD5_1N |
| RN2 | 6 | TMD5_1P |
| RN2 | 7 | TMD5_2N |
| RN2 | 8 | TMD5_2P |



External Connection

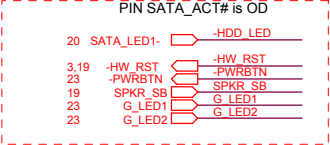


VGA

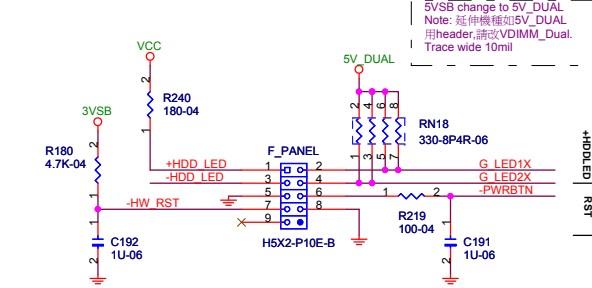


FRONT PANEL

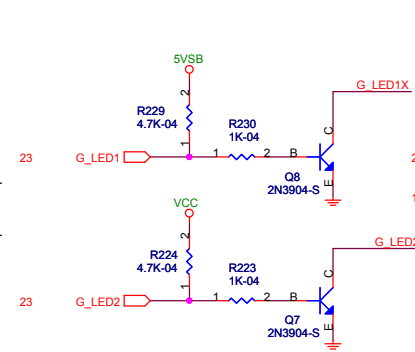
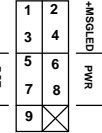
External Connection



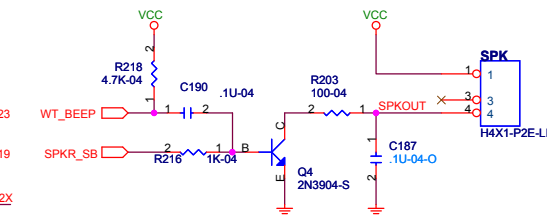
If you found anything wrong with this circuit,please contact with Jack Hu (Ext:622)



F_PANEL

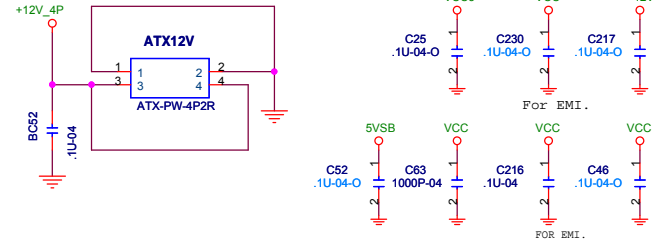
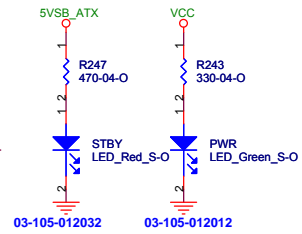
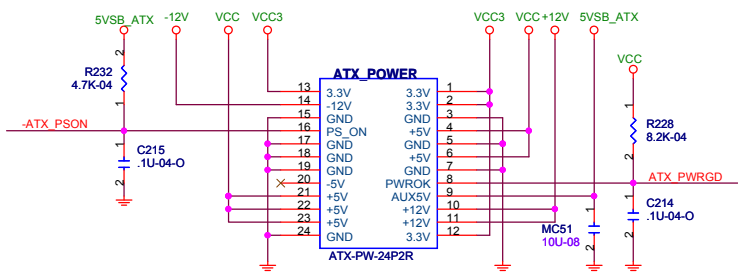
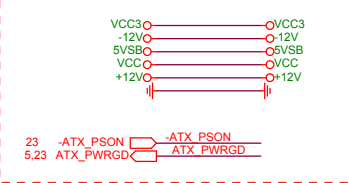


BUZZER



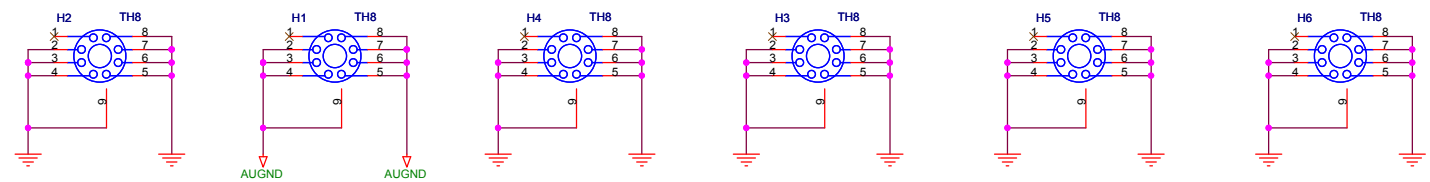
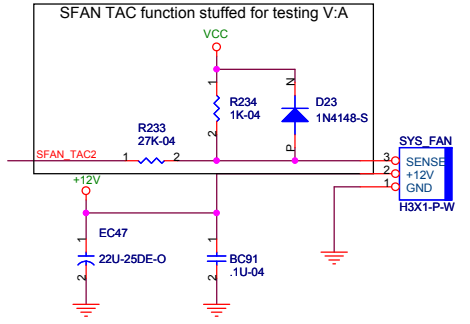
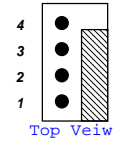
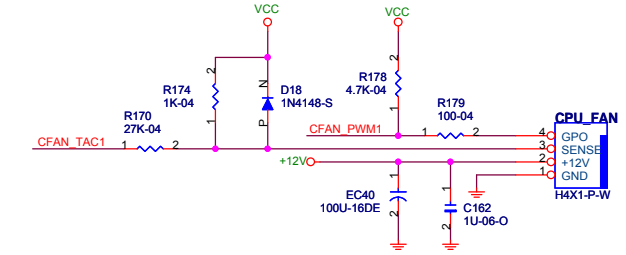
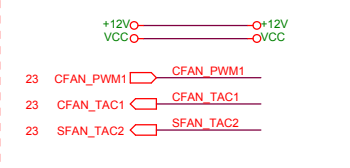
POWER CONNECTOR

External Connection

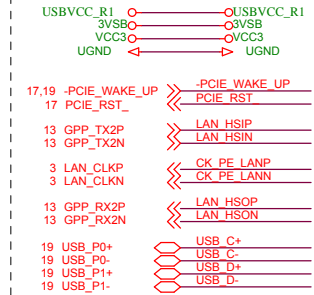


FAN

External Connection



External Connection



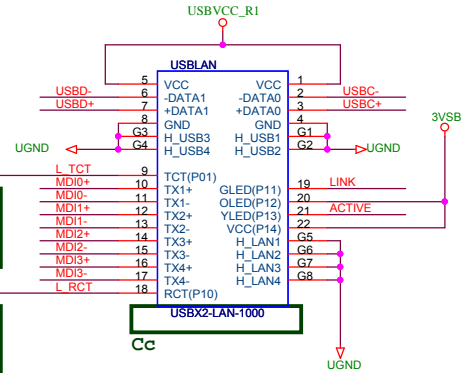
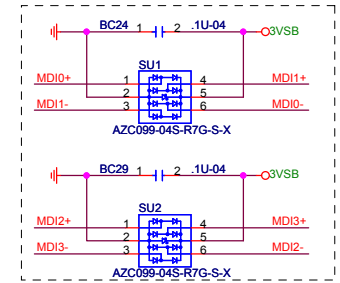
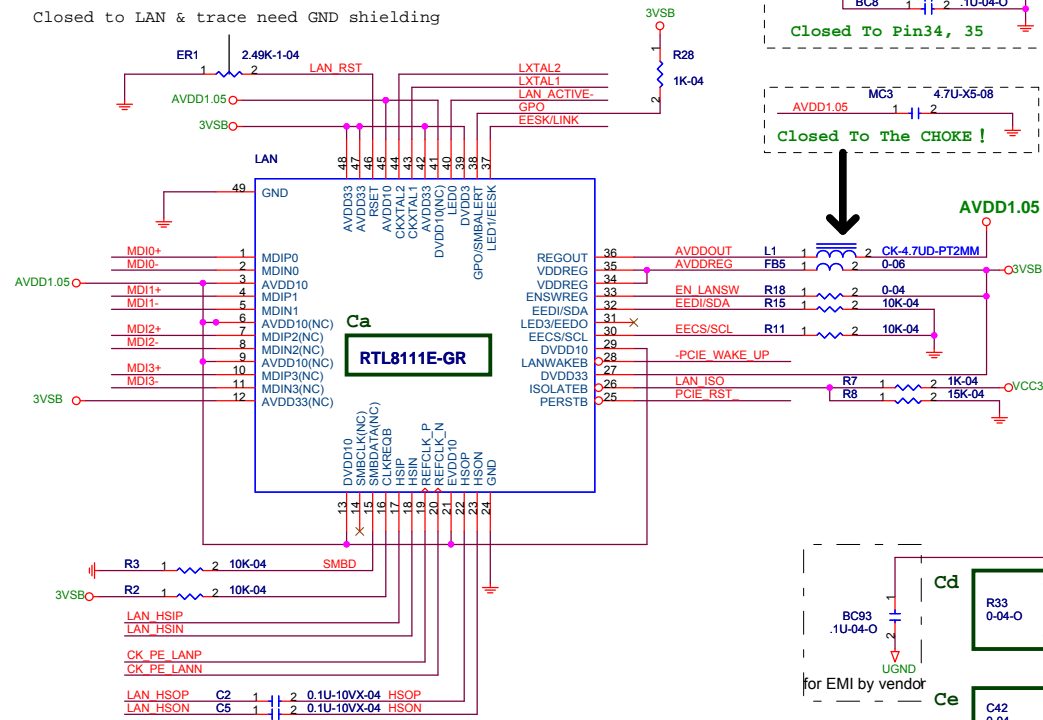
新手提醒:

LAN_HSOP/N請接到SB的PCIE RX端

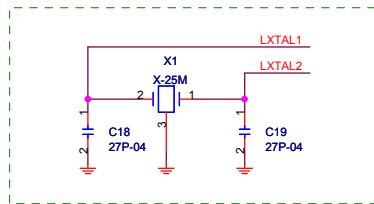
LAN_HSIP/N請接到SB的PCIE TX端

LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

Closed to LAN & trace need GND shielding



Link: Green on
Active: Yellow blinking

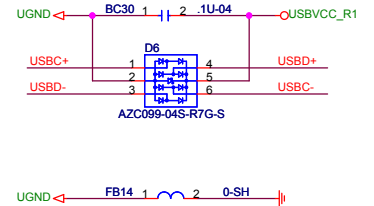
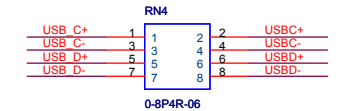
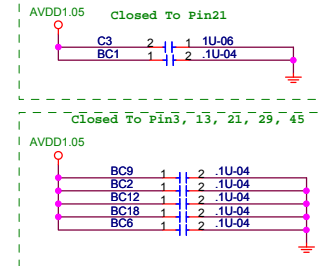
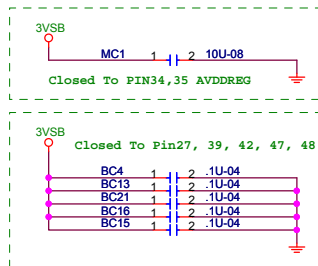
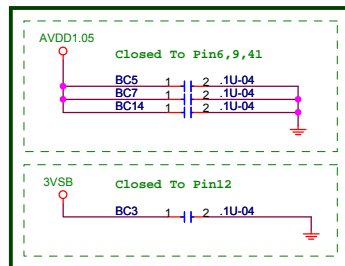


BOM Difference

| | RTL8111E-GR 1000M | RTL8105E-GR 10/100M |
|----|----------------------|------------------------|
| Ca | RTL8111E-GR | RTL8105E-GR |
| Cb | V | X |
| Cc | USBX2-LAN-1000 | USBX2-LAN-100 |
| Cd | X | V |
| Ce | 0-04 | .01U-04 |
| Cf | | |
| Cg | | |

Default

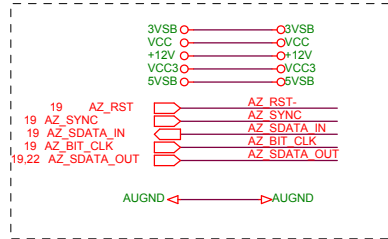
Cb



AZC099-04S-R7G-S

UGND FB14 1 2 0-SH

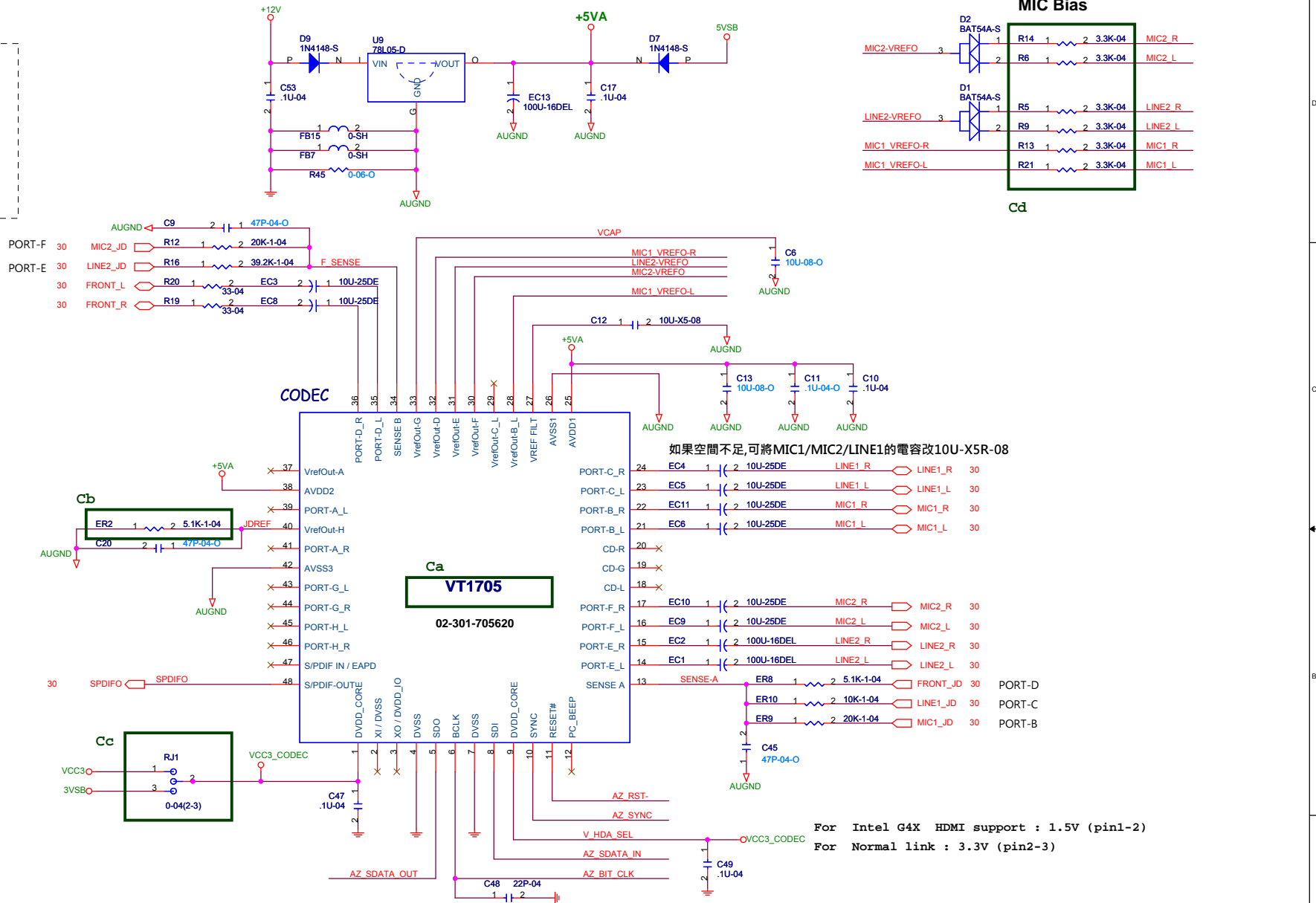
External Connection



BOM Difference

| Location | ALC662 | VT1705 |
|----------|---------------|-----------|
| Ca | ALC662-VC-GRS | VT1705 |
| Cb | 20K-1-04 | 5.1K-1-04 |
| Cc | ARJ2(1-2) | ARJ2(2-3) |
| Cd | 2.2K-04 | 3.3K-04 |
| Ce | 75-04 | 16-04 |

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

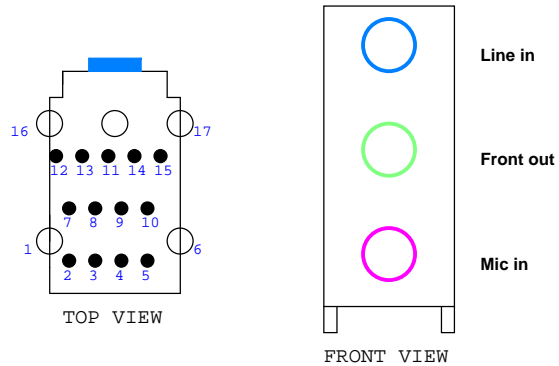
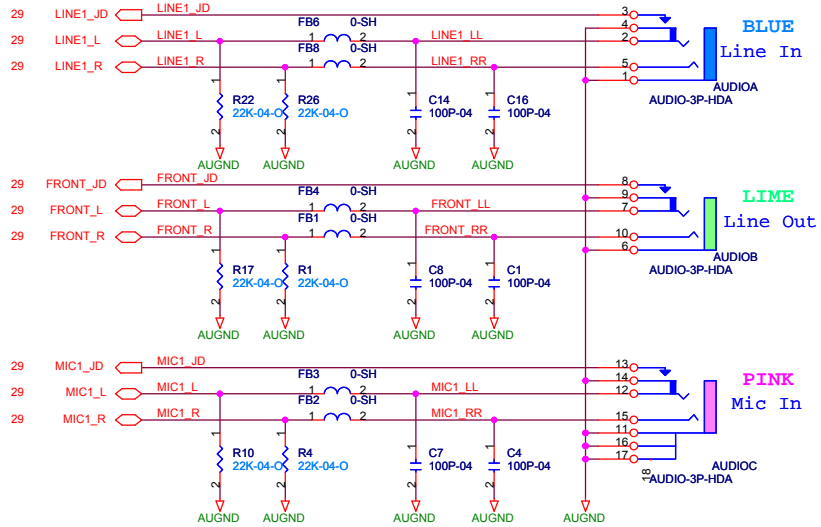


External Connection

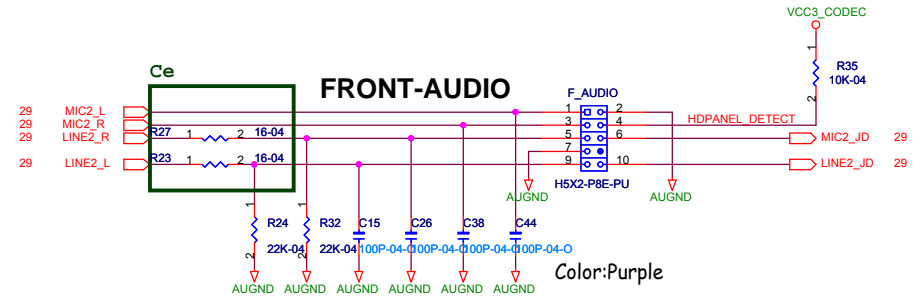
19 HDPANEL_DETECT  HDPANEL_DETECT

* HDPANEL_DETECT connect to SIO or SB GPIO for AC97 Panel support

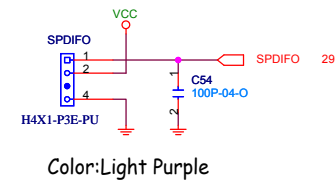
REAR-AUDIO

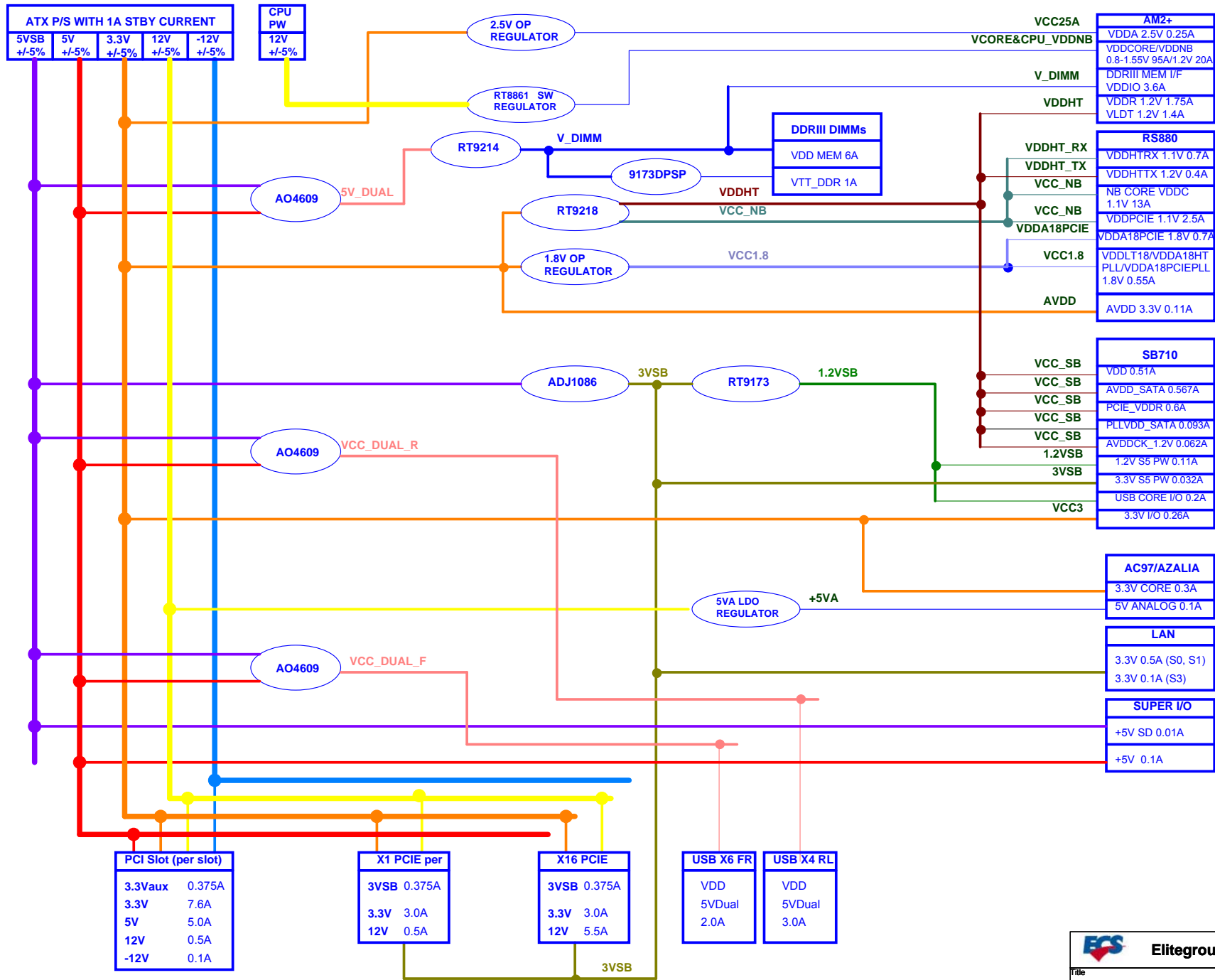


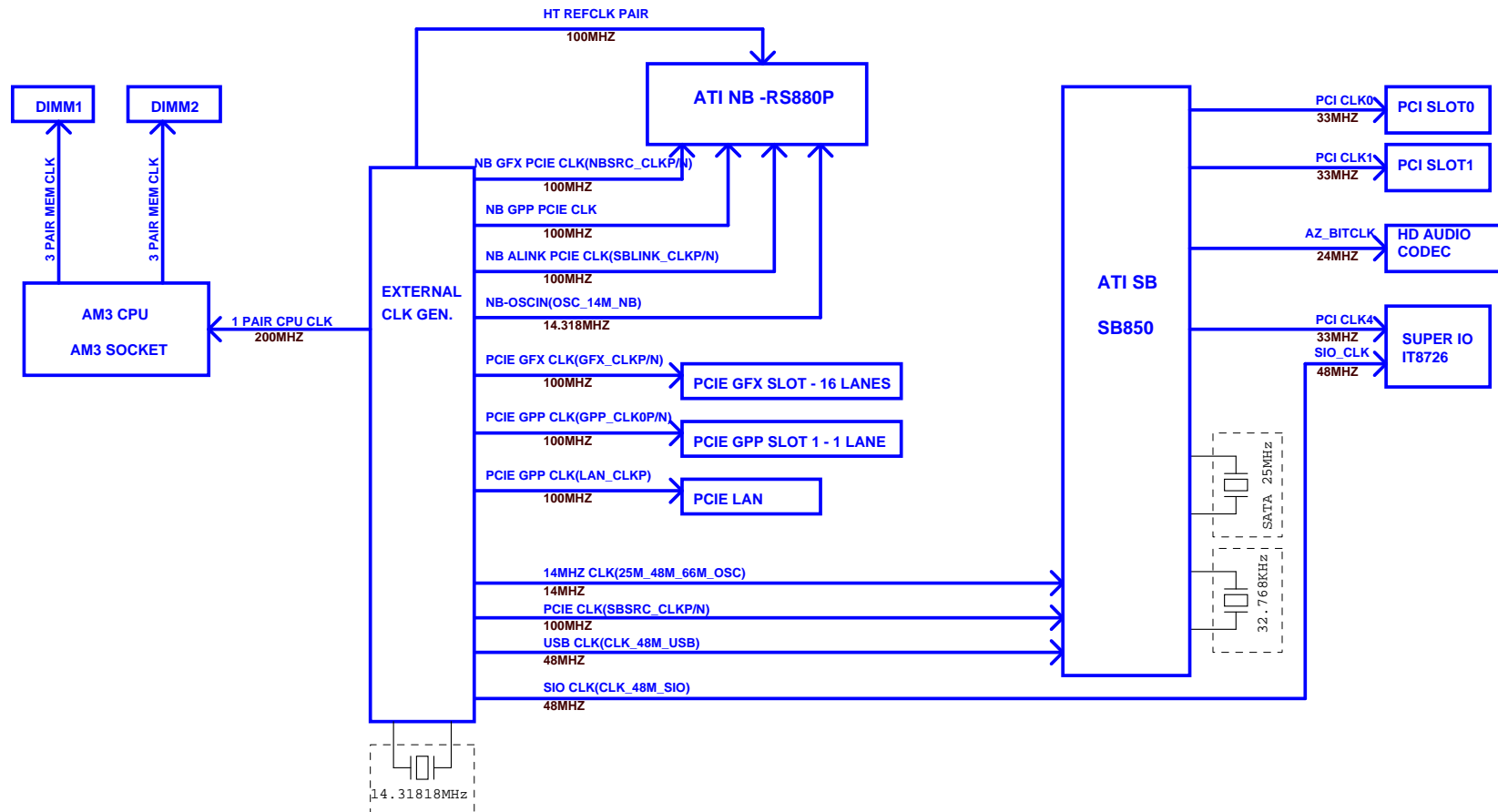
FRONT-AUDIO



SPDIF-OUT







Power Sequence

